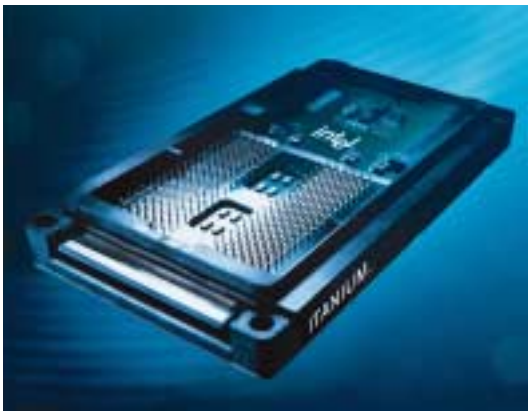
Intel® Itanium™ Processor at 800 MHz and 733 MHz Datasheet

Product Features

- Wide parallel hardware based on Itanium™ architecture for high performance
  - —Fifteen execution units
  - —Cache hints for L1, L2, and L3 caches for reduced memory latency
  - —256 general and floating-point registers with rotating registers
  - —Register stack engine for effective management of processor resources
  - —Support for predication and speculation
  - —Full speed 4-MB or 2-MB L3 cache
  - —On-die L1 and L2 caches
- Extensive RAS features for mission-critical applications
  - —Full SMBus compatibility
  - —Enhanced Machine Check Architecture with ECC and parity error recovery
  - —Built-in processor information ROM
  - —Built-in programmable EEPROM
- High bandwidth system bus for multiprocessor scalability
  - —2.1 GB/s bandwidth
  - —64-bit wide system bus
  - —44 bits of physical memory addressing, and 54 bits of virtual addressing
  - —Up to four processors on the same system bus at 266 MHz data frequency
  - —Expandable to systems with multiple system buses
  - —Compatible with Intel® 460GX chipset
- Features to support flexible platform environments
  - —Hardware compatible with IA-32 binaries
  - —Bi-endian support
  - —Processor Abstraction Layer eliminates processor dependencies

The Intel® Itanium™ processor, the first in a family of processors based on Itanium architecture, is designed to address the needs of high-performance servers and workstations. The Itanium architecture goes beyond RISC and CISC approaches by pairing massive processing resources with intelligent compilers that enable parallel execution explicit to the processor. Its large internal resources combine with predication and speculation to enable optimization for high performance applications running on Windows* Advanced Server Limited Edition, Windows* XP 64-bit Edition, Linux, HP-UX* 11i v1.5 and other Itanium-based operating systems. The Itanium processor is designed to support very large scale systems, including those employing several thousand processors, to provide the processing power and performance head room for back-office data-intensive servers, internet servers, and large data set computation intensive applications for high-end workstations. SMBus compatibility and comprehensive Reliability, Availability and Serviceability (RAS) features make the Itanium processor ideal for applications that demand continuous operation. In addition, the Itanium processor is fully compatible, in hardware, with IA-32 instruction binaries to preserve existing software investments. For high performance servers and workstations, the Itanium processor offers outstanding performance and reliability for today's applications and the scalability to address the growing e-business needs of tomorrow.



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Revision History

Version Number	Description	Date
001	Initial Release of this document.	May 2001
002	Updated Coversheet.	August 2001

Introduction 1

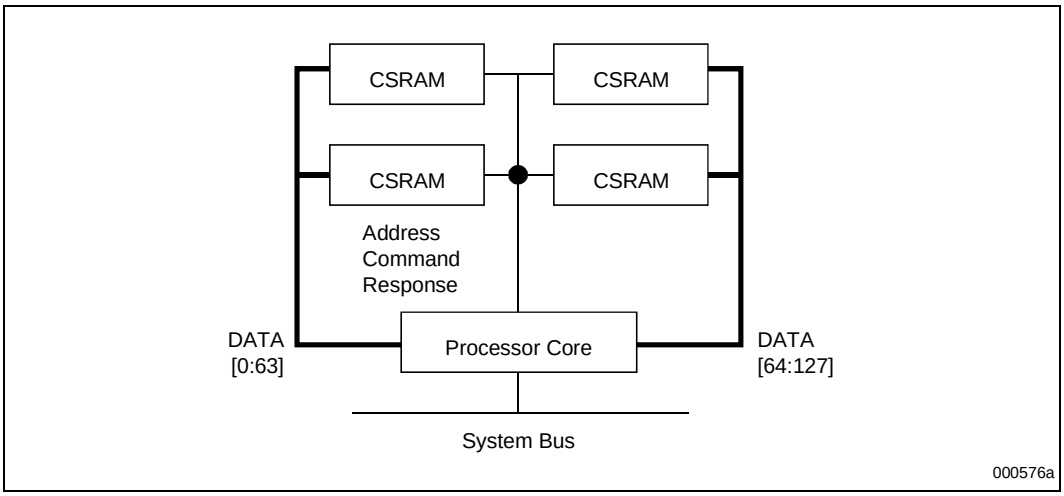
The Intel® Itanium™ processor is the first member of a family of processors based on the 64-bit Itanium architecture. The Itanium architecture provides high performance and 64-bit architecture in addition to full binary compatibility with IA-32 software. This document provides the electrical, mechanical, thermal and system management feature specifications for the Intel Itanium processor cartridge for use while designing systems with the Intel Itanium processor.

Note: This document contains data that is subject to change. Intel shall have no responsibility for conflicts or incompatibilities arising from future changes to the data contained in this document.

1.1 Intel® Itanium™ Processor 4 MB Cartridge

The Intel Itanium processor 4 MB cartridge contains the processor core and 4 MB of Level 3 (L3) cache (four 1 MB Intel Cache SRAM). The high speed L3 cache bus is completely isolated in the Intel Itanium processor cartridge. Figure 1-1 shows the block diagram for the Intel Itanium processor 4 MB cartridge.

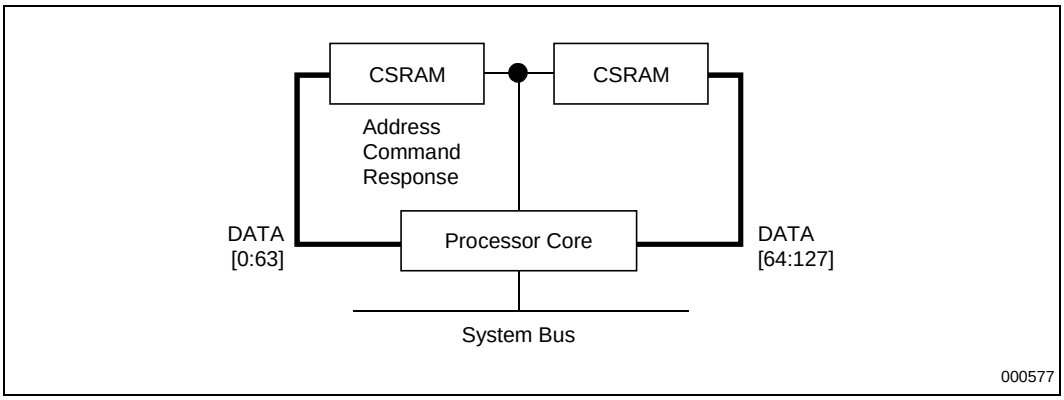
Figure 1-1. Intel® Itanium™ Processor 4 MB Cartridge Block Diagram



1.2 Intel® Itanium™ Processor 2 MB Cartridge

The Intel Itanium processor 2 MB cartridge contains the processor core and 2 MB of L3 cache (two 1 MB Intel Cache SRAMs). The high speed L3 cache bus is completely isolated in the Intel Itanium processor cartridge. Figure 1-2 shows the block diagram for the Intel Itanium processor 2 MB cartridge.

Figure 1-2. Intel® Itanium™ Processor 2 MB Cartridge Block Diagram



1.3 Intel® Itanium™ Processor System Data Bus

The system bus signals use an enhanced version of the low voltage GTL+ (Gunning Transceiver Logic) signaling technology used by the Pentium® III and Pentium III Xeon™ processors. For the highest performance, the system bus supports source synchronous data transfers. The system bus signals require external termination on each end of the signal trace to help supply the high signal level and to control reflections on the transmission line. Maximum system data bus throughput is 2.1 GB/sec.

1.4 Processor Abstraction Layer

The Itanium processor cartridge functionality requires the Processor Abstraction Layer (PAL) firmware. This PAL firmware resides in the system flash memory and is part of the Intel Itanium architecture. This firmware provides an abstraction level between the processor hardware implementation, the system software and platform firmware to maintain a single software interface for multiple implementations of the processor silicon steppings. PAL firmware encapsulates those processor functions that may change from one implementation to another so that the System Abstraction Layer (SAL) can maintain a consistent view of the processor.

SAL consists of the platform dependent firmware. SAL is the Basic Input/Output System (BIOS) required to boot the operating system (OS). The *Intel® Itanium™ Architecture Software Developer's Manual*, Vol. 2: System Architecture describes the PAL interface in detail.

1.5 Mixing Processors of Different Frequencies and Cache Sizes

All Itanium processors on the same system bus are required to have the same cache size (either 2 M or 4 M) and identical core frequency. Mixing components of different core frequencies and cache sizes is not supported and has not been validated by Intel. Operating system support for multi-processing with mixed components should also be considered.

While Intel has done nothing to specifically prevent processors within a multi-processor environment from operating at differing frequencies and differing cache sizes, there may be

uncharacterized errata that exist in such configurations. Customers would be fully responsible for, and may wish to perform, validation of system configurations with mixed components other than the supported configurations described above.

1.6 Terminology

In this document, a '#' symbol after a signal name refers to an active low signal. This means that a signal is in the active state (based on the name of the signal) when driven to a low level. For example, when RESET# is low, a processor reset has been requested. When NMI is high, a non-maskable interrupt has occurred. In the case of lines where the name does not imply an active state but describes part of a binary sequence (such as address or data), the '#' symbol implies that the signal is inverted. For example, D[3:0] = 'HLHL' refers to a hex 'A', and D [3:0] # = 'LHLH' also refers to a hex 'A' (H= High logic level, L= Low logic level).

The term 'system bus' refers to the interface between the processor, system core logic and other bus agents. The system bus is a multiprocessing interface to processors, memory and I/O. The L3 cache does NOT connect to the system bus, and is not accessible by other agents on the system bus. Cache coherency is maintained with other agents on the system bus through the MESI cache protocol as supported by the HIT# and HITM# bus signals.

The term "Intel Itanium processor" refers to the cartridge package which interfaces to a host system board through a PAC418 connector. Intel Itanium processors include a processor core, an L3 cache, and various system management features. The Intel Itanium processor includes a thermal plate for a cooling solution attachment.

A signal name has all capitalized letters, e.g. VCTERM.

A symbol referring to a voltage level, current level, or a time value carries a plain subscript, e.g., VCC_{core}, or a capitalized abbreviated subscript, e.g. T_{CO}.

1.7 References

The reader of this specification should also be familiar with material and concepts presented in the following documents and tools:

- *Intel® Itanium™ Processor Hardware Developer's Manual* (Document Number: 248701)
- *Intel® Itanium™ Processor Specification Update* (Document Number: 249720)
- *PAC418 VLIF Socket and Cartridge Ejector Design Specifications*
- *PAC418 Cartridge/Power Pod Retention Mechanism and Triple Beam Design Guide*
- *Itanium™ Processor Heatsink Guidelines*
- *Itanium™ Processor VTT Voltage Regulation Specification*
- *Intel® Itanium™ Architecture Software Developer's Manual, Volume 1-4* (Document Numbers: 245317, 245318, 245319, and 245320)

Note: Contact your Intel representative for the latest revision of the documents without document numbers.

Electrical Specifications 2

This chapter describes the electrical specifications of the Intel Itanium processor 4-MB and 2-MB cartridges.

2.1 Intel® Itanium™ Processor System Bus

Most Intel Itanium processor signals use a variation of the Pentium III processor and Pentium III Xeon processor AGTL+ signaling technology. The termination voltage, VCTERM, is generated on the baseboard and is the system bus high reference voltage. The buffers that drive most of the system bus signals on the Intel Itanium processor are actively driven to VCTERM during the low-to-high transition to improve rise times and reduce noise. These signals should still be considered open-drain and require termination to VCTERM which provides the high signal level. This specification is slightly different from the standard AGTL+ specification.

AGTL+ inputs use differential receivers which require a reference signal (VREF). VREF is used by the receivers to determine if a signal is a logical 0 or a logical 1. The Intel Itanium processor uses separate address, control and data VREFs which are generated on the baseboard. Termination is used to pull the bus up to the high voltage level and to control signal integrity on the transmission line. The baseboard contains termination resistors that provide termination for each of the Intel Itanium processor system bus signals. These specifications assume the equivalent of five AGTL+ loads (four processors and one chipset) to ensure the proper timings on rising and falling edges.

2.1.1 System Bus Power Pins

There are 26 VCTERM PAC418 input pins to provide power to the driver buffers and termination during a low-to-high signal transition. There are 140 VSS pins which, in addition to the $VSS_{processor}$ input at the power tab connector, provide ground to the processor and cache. Power for the processor core, cache core and cache I/O is provided through the power tab connector by $VCC_{processor}$ and VCC_{cache}. Two 3.3V pins are provided on the system bus for use by the SMBus. 3.3V, VCTERM, and VSS must remain electrically separated from one another.

2.1.2 System Bus Reserved Pins

All pins designated as “N/C” or “No Connect” should remain unconnected. Pins designated as “PU[2:0]” or “PD[3:0]” should be connected via a resistor to VCTERM or VSS, respectively (see Section 2.8 for details). The pins must be strapped to the appropriate voltage for normal operation.

2.2 System Bus Signals

2.2.1 Signal Groups

Table 2-1 contains Intel Itanium processor system bus signals that have been combined into groups by buffer type and whether they are inputs, outputs or bidirectional.

All system bus outputs should be treated as open drain and require a high level source provided externally by the termination resistor.

AGTL+ inputs have differential input buffers which use 2/3 VCTERM as a reference level. AGTL+ output signals require termination to VCTERM. In this document, “AGTL+ Input Signals” refers to the AGTL+ input group as well as the AGTL+ I/O group when receiving. Similarly, “AGTL+ Output Signals” refers to the AGTL+ output group as well as the AGTL+ I/O group when driving.

The Power Good signal and TAP (Test Access Port) Connection Input signals use a non-differential receiver with levels that are similar to AGTL+. No reference voltage is required for these signals. The TAP Connection Output signals are AGTL+ output signals.

The HSTL Clock signals are the differential clock inputs for the Intel Itanium processor. The System Management Bus (SMBus) signals and LVTTL Power Pod signals are driven using the 3.3V CMOS logic levels listed in Table 2-8 and Table 2-9, respectively. Please refer to Section 2.2.2 for descriptions for the “Other” and “Reserved” signals.

Please refer to the *Intel® Itanium™ Processor Hardware Developer’s Manual* for recommended terminations for all system bus signals.

Table 2-1. Intel® Itanium™ Processor System Bus Signal Groups

Group Name	Signals
AGTL+ Input Signals	BPRI#, BR[3:1]#, DEFER#, GSEQ#, ID[7:0]#, IDS#, RESET#, RS[2:0]#, RSP#, TRDY#
AGTL+ Asynchronous Interrupt Input Signals[a]	A20M#, DRATE#, IGNNE#, INIT#, LINT[1,0], PMI#, TRISTATE#
AGTL+ Output Signals	FERR#, THERMTRIP#
AGTL+ I/O Signals	A[43:3]#, ADS#, AP[1:0]#, BERR#, BINIT#, BNR#, BPM[5:0]#, BR0#, D[63:0]#, DBSY#, DEP[7:0]#, DRDY#, HIT#, HITM#, LOCK#, REQ[4:0]#, RP#, SBSY#, STBN[3:0]#, STBP[3:0]#, TND#
Power Good Signal	PWRGOOD
HSTL Clock Signals	BCLKN, BCLKP
TAP Connection Input Signals	TCK, TDI, TMS, TRST#
TAP Connection Output Signals	TDO
System Management Signals	3.3V, SMA[2:0], SMSC, SMSD, SMWP, THRMALERT#
Power Signals	GND, VCTERM, VREFA[1:0], VREFC[1:0], VREFDL[1:0], VREFDR[1:0]
LVTTL Power Pod Signals	OUTEN, PPODGD#
Other	TUNER[2:1], PROCPRES#
Reserved	N/C, PD[3:0], PU[2:0]

a. The AGTL+ asynchronous interrupt signals have special setup and hold timings that differ from those of standard AGTL+. See Table 2-12 for more information.

2.2.2 Signal Descriptions

The *Intel® Itanium™ Processor Hardware Developer’s Manual* document contains functional descriptions of all system bus signals and LVTTL Powerpod signals. Further descriptions of the System Management signals are contained in Chapter 6. The signals listed under the group “Power” and “Other” are described here.

Table 2-2. Signal Descriptions

Group Name	Signals
GND	System ground
N/C	No connection can be made to these pins.
PD[3:0]	These pins must be connected to VSS through a 1 KΩ resistor.
PU[2:0]	PU2 and PU0 must be connected to VCTERM through a 1 KΩ resistor. PU1 must be connected to VCTERM through a 100 Ω resistor.
TUNER[2:1]	A reference resistor must be connected between each pin to GND. The reference resistors determine driver buffer impedance and slew rate settings for the processor.
PROCPRES#	This pin must be connected to VCTERM through a 10 KΩ resistor on the system board.
VCTERM	System bus termination voltage (see Table 2-3)
VREFA[1:0]	Reference voltage inputs to the address signal receiver buffers.
VREFC[1:0]	Reference voltage inputs to the control signal receiver buffers.
VREFDL[1:0], VREFDR[1:0]	Reference voltage inputs to the data signal receiver buffers.

2.3 Cartridge Specifications

Table 2-3 list the DC voltage, current and power specifications for the Intel Itanium processor 2-MB and 4-MB cartridges. The voltage and current specifications are defined at the Intel Itanium processor PAC418 cartridge pins.

Operational specifications listed in Table 2-3 through Table 2-16 are only valid while meeting specifications for case temperature, clock frequency, and input voltages.

Note: Care should be taken to read all notes associated with each parameter.

Table 2-3. Intel® Itanium™ Processor 2-MB and 4-MB Cartridge Specification

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VCC_{core_st}	Static tolerance for VCC_{core}	$VID_{processor}$ -5%	$VID_{processor}$	$VID_{processor}$ +5%	V	
VCC_{core_tr}	Transient tolerance for VCC_{core}	$VID_{processor}$ -6%	$VID_{processor}$	$VID_{processor}$ +7%	V	
VCC_{cache_st}	Static tolerance for VCC_{cache}	VID_{cache} -5%	VID_{cache}	VID_{cache} + 5%	V	
VCC_{cache_tr}	Transient tolerance for VCC_{core}	VID_{cache} -6%	VID_{cache}	VID_{cache} + 7%	V	
VCTERM	Termination voltage	1.5-1.5%	1.5	1.5+1.5%	V	
3.3V	VCC for SMBus components	3.14	3.30	3.47	V	

Table 2-3. Intel® Itanium™ Processor 2-MB and 4-MB Cartridge Specification (Cont'd)

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VREFA[1:0], VREFC[1:0], VREFDL[1:0] VREFDR[1:0]	Reference voltage		2/3*VCTERM		V	
ICC_{core}	Current for the processor core	1.0		71.4	A	a, b, c
ICC_{cache}	Current for the cache	1.0		16.5	A	a, b, c
ICC_{TERM}	Termination voltage current		0.25	0.5	A	d
$PS_{processor}$	Power supply slew rate at the processor power connector tab			0.4	A/ns	
PS_{cache}	Power supply slew rate at the cache power tab connector			0.1	A/ns	
PS_{CTERM}	Termination voltage slew rate at the PAC418 pins			0.05	A/ns	
PWR_{max}	Maximum 2M cartridge power Maximum 4M cartridge power			116 130	W	c
PWR_{TDP}	Thermal design power 4MB Cartridge 2MB Cartridge			116-130 130 116	W	e

a. Maximum current (ICC) specifications are intended for system power supply design. The maximum current is defined based on worst-case VCC, temperature and software application mix.
b. Maximum ICC_{core} and ICC_{cache} do not occur simultaneously.
c. For all core frequencies.
d. Current drawn by the I/O stage of the processor through the VCTERM pin, not through the termination resistor.
e. Maximum thermal design power is an estimate of the power dissipation for the Intel® Itanium™ processor while executing a worst-case application mix under nominal VCC and worst-case temperature.

2.4 Signal Specifications

2.4.1 DC Specifications

This section describes the DC specifications of the system bus signals. The processor signals DC specifications are defined at the Intel Itanium processor core. Each signal trace between the Intel Itanium processor PAC418 cartridge pin and the processor core carries a small amount of current and has a finite resistance. The signal current produces a voltage drop between the cartridge pin and the core. Simulations should be run in accordance with these specifications to the processor core.

Table 2-4 through Table 2-9 describe the DC specifications for the AGTL+, PWRGOOD, HSTL Clock, TAP Connection, System Management, and LVTTL signals. Please refer to the *Intel® Itanium™ Processor Hardware Developer's Manual* for the TAP connection signals DC specifications at the debug port. The signals VREFA[1:0], VREFC[1:0], VREFDL[1:0] and VREFDR[1:0] are collectively referred to as VREF.

Table 2-4. AGTL+ Signals DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	–0.3	V_{REF} – 200 mV	V	
V_{IH}	Input High Voltage	V_{REF} + 200 mV	$VCTERM_{max}$	V	
V_{OL}	Output Low Voltage		0.6	V	a
I_{OL}	Output Low Current @ 0.5V	50		mA	
I_L	Leakage Current		± 100	µA	b
C_{AGTL+}	AGTL+ Pin Capacitance		7	pF	c

a. Parameter measured into a 20-ohm resistor to VCTERM.
b. At 1.5V ±3%.
c. Total of I/O buffer with ESD structure, package parasitics and capacitance for socket.

Table 2-5. PWRGOOD Signal DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	–0.3	0.35	V	
V_{IH}	Input High Voltage	1.2	$VCTERM_{max}$	V	

Table 2-6. System Bus Clock Differential HSTL DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{IH}	Input High Voltage	0.78		1.7	V	Min=$V_{X,min}$+0.1
V_{IL}	Input Low Voltage	–0.3		0.58	V	Max=$V_{X,min}$-0.1
V_X	Input Crossover Voltage	0.68		0.9	V	

Table 2-7. TAP Connection Signals DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	–0.3	0.5	V	
V_{IH}	Input High Voltage	1.2	$VCTERM_{max}$	V	
V_{OL}	Output Low Voltage		0.3	V	a
I_{OL}	Output Low Current	16.5	19.8	mA	

a. Parameter measured into a 20-ohm resistor to VCTERM.

Table 2-8. SMBus Signals DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{IL}	Input Low Voltage	–0.3		0.3*3.3V	V	
V_{IH}	Input High Voltage	0.7*3.3V		3.465	V	Max=3.3+5%
V_{OL}	Output Low Voltage			0.4	V	
$I_{3.3V}$	3.3V Supply Current		5.0	10.0	mA	
I_{OL}	Output Low Current			3	mA	a
I_{OL2}	Output Low Current	6			mA	b
I_{LI}	Input Leakage Current			10	µA	
I_{LO}	Output Leakage Current			10	µA	

a. The value specified for I_{OL} applies to all signals except for THRMALERT#.
b. The value specified for I_{OL2} applies only to THRMALERT# which is an open drain signal.

Table 2-9. LVTTL DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage		0.8	V	
V_{IH}	Input High Voltage	2.0	3.63	V	Max=3.3+10%
V_{OL}	Output Low Voltage		0.4	V	
V_{OH}	Output High Voltage	2.4		V	

2.4.2 AC Specifications for the System Bus

The system address bus operates at a clock frequency of 133 MHz. The system data bus uses source synchronous clocking, allowing 266 MHz operation.

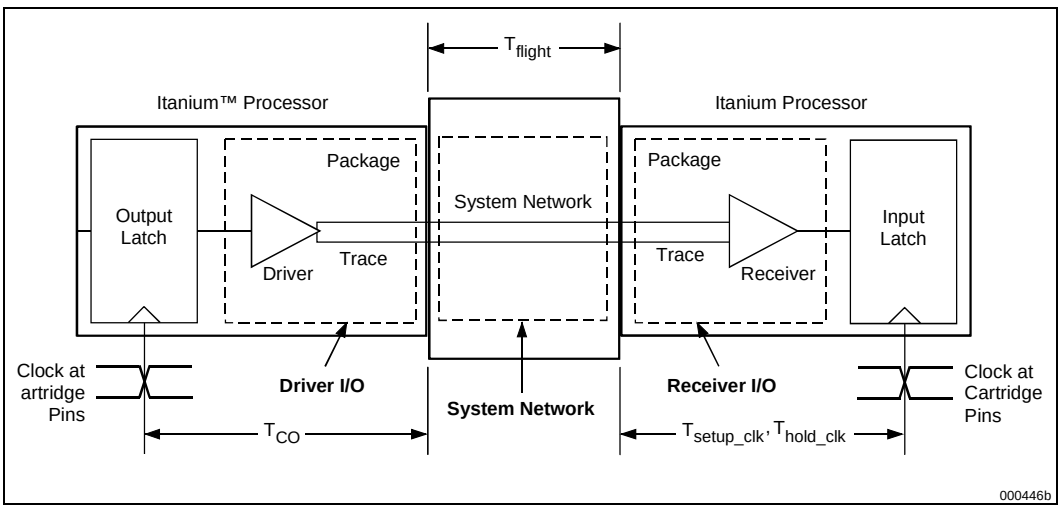
The AC timing specifications in this section are shown with respect to the pins of the component. The intent is to provide a method for verifying the component's I/O timings in a real system. These specifications reflect the I/O timing specifications against which the actual component can be tested in a system environment under worst case conditions.

2.4.2.1 Common Clock AC Timing Specifications

The common clock timing specifications for the system bus consists of three parts: clock to driver output delay (T_{CO}), flight time (T_{flight}), and receiver setup and hold to bus clock (T_{setup} and T_{hold}). These timing parameters reference the driver and receiver components at the pin and are intended for verifying the component's I/O timings in a real system.

Figure 2-1 illustrates these timing specifications.

Figure 2-1. Common Clock Timing Definition Overview

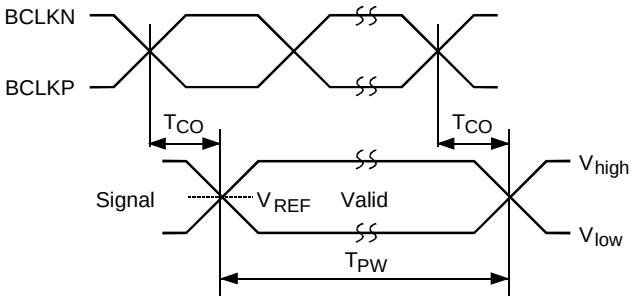


2.4.2.1.1 Clock to Driver Output Delay

The clock to driver output delay (T_{CO}) is defined as the time between the differential bus clock crossing at the input pin (at the driving agent) relative to the signal crossing a voltage reference, V_{REF}, at the output pin (of the driving agent) at an edge rate defined by the environment conditions.

Figure 2-2 illustrates the T_{CO} timing definition, and Table 2-10 and Table 2-11 list the T_{CO} values for the common clock system bus signals. $T_{CO,min}$ represents the delay under fast conditions and $T_{CO,max}$ represents the delay under slow conditions.

Figure 2-2. Common Clock Mode Valid Delay Timings



T_{CO} = Clock-to-output delay

T_{PW} = Pulse width

V_{REF} = V_{REF} for AGTL + signal group

V_{high} = AGTL + signals must achieve a DC high level of at least V_{REF} +200 mV

V_{low} = AGTL + signals must achieve a DC low level of at least V_{REF} –200 mV

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2.4.2.1.2 Flight Time

The flight time (T_{flight}) is defined as the time between the signal crossing a reference voltage, V_{REF}, at the output pin (of the driving agent) relative to the signal crossing V_{REF} at the input pin (of the receiving agent). Flight time is a system dependent timing based on the specific PCB technology, the interface routing topology, and applicable connectors.

2.4.2.1.3 Receiver Setup and Hold to Bus Clock

The receiver setup and hold to bus clock (T_{setup} and T_{hold}) is defined by the signal at the input pin (of the receiving agent) crossing a reference voltage, V_{REF}, relative to the differential bus clock crossing at the input pin (of the receiving agent). T_{setup} and T_{hold} each include the internal clock skew and tester guardband.

Figure 2-3 illustrates the T_{setup} and T_{hold} timing definition, and Table 2-10, Table 2-11, and Table 2-12 list the T_{setup} and T_{hold} values for the common clock system bus signals. T_{setup} represents the worst case setup time requirement under slow conditions. T_{hold} represents the worst case hold time requirement under fast conditions.

Table 2-10 show the common clock AC timing parameters that the actual component is tested to in a system environment under worst case conditions. These parameters are intended to provide a method for verifying the component's I/O timings in an actual system. All timings are specified in nanoseconds (ns) to the pin of the component at a rated load of 20Ω. The voltage reference is V_{REF}.

Figure 2-3. Common Clock Mode Setup and Hold Timings

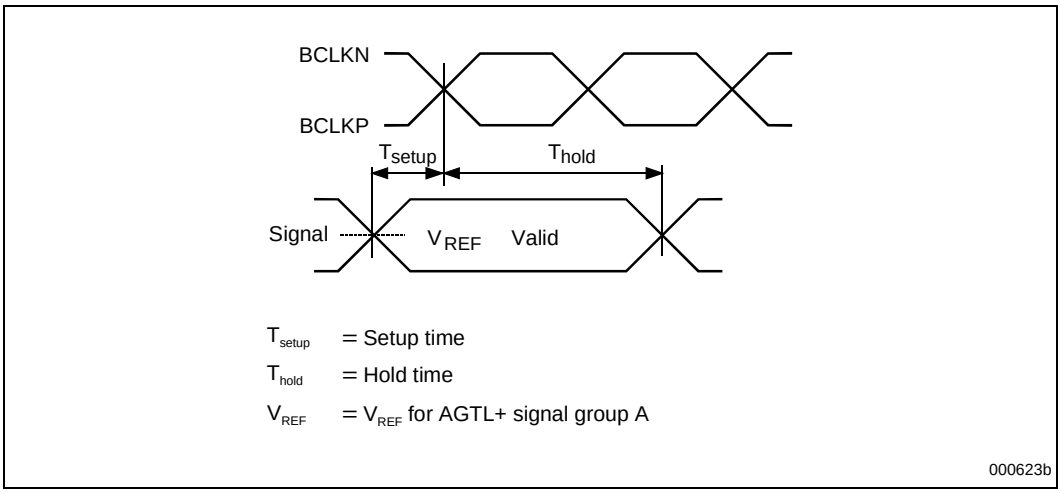


Table 2-10. AGTL+ Address/Control Signal Group Common Clock AC Timing Specifications

Symbol	Parameter	Min	Max	Unit	Figure	Notes
T_{CO}	Output H → L Clock to Output Delay	0.43	3.46	ns	2-2	a
$T_{CO,BNR\#}$	Output H → L Clock to Output Delay	0.43	3.96	ns	2-2	b
T_{CO}	Output L → H Clock to Output Delay	0.64	3.14	ns	2-2	a
T_{setup}	Input Setup Time before BCLK	1.62		ns	2-3	
T_{hold}	Input Hold Time after BCLK	1.00		ns	2-3	

a. Delay timings are specified into an idealized 20-ohm resistor to VCTERM.
b. Delay timings are specified into an idealized 20-ohm resistor to VCTERM, for BNR# signal only.

Table 2-11. AGTL+ Data Signal Group Common Clock AC Timing Specifications

Symbol	Parameter	Min	Max	Unit	Figure	Notes
T_{CO}	Output H → L Clock to Output Delay	0.53	2.85	ns	2-2	a
T_{CO}	Output L → H Clock to Output Delay	0.71	3.01	ns	2-2	a
T_{setup}	Input Setup Time before BCLK	1.62		ns	2-3	
T_{hold}	Input Hold Time after BCLK	1.00		ns	2-3	

a. Delay timings are specified into an idealized 20-ohm resistor to VCTERM.

Table 2-12. AGTL+ Asynchronous Interrupt Signal Group Common Clock AC Specifications

Symbol	Parameter	Min	Max	Unit	Figure	Notes
T_{setup}	Input Setup Time before BCLK	1.034		ns	2-3	a
T_{hold}	Input Hold Time after BCLK	1.000		ns	2-3	a
T_{PW}	Input Pulse Width	1		BCLK		

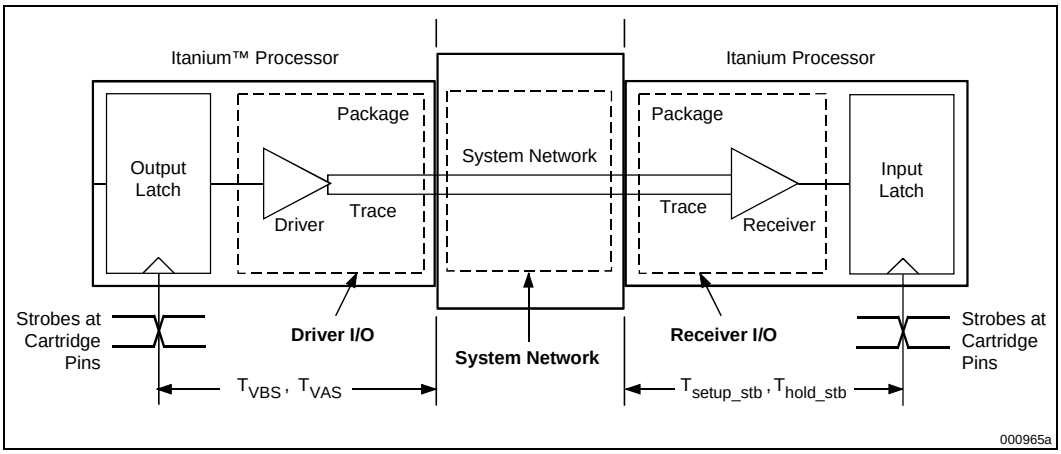
a. These signals can be driven asynchronously, but to guarantee determinism, these setup and hold times must be met at the processor.

2.4.2.2 Source Synchronous AC Timing Specifications

The source synchronous timing specifications for the system bus consists of three parts: driver valid before and after strobe (T_{VBS} and T_{VAS}), delta flight time (ΔT_{flight}), and receiver setup and hold to strobe (T_{setup} and T_{hold}). These three timing parameters reference the driver and receiver components at the pin and are intended for verifying the component's I/O timings in a real system.

Figure 2-4 illustrates these timing specifications.

Figure 2-4. Source Synchronous Timing Definition Overview

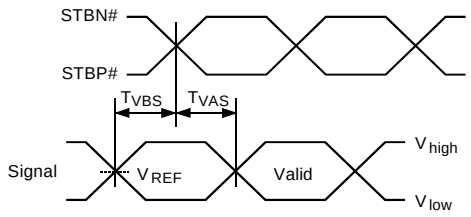


2.4.2.2.1 Driver Valid Before and After Strobe

The driver valid before and after strobe (T_{VBS} and T_{VAS}) is defined as the time between the signal crossing a reference voltage, V_{REF}, at the output pin (of the driving agent) relative to the differential strobe crossing at the output pin (of the driving agent).

Figure 2-5 illustrates the T_{VBS} and T_{VAS} timing definition and Table 2-13 lists the T_{VBS} and T_{VAS} values for the source synchronous system bus signals. T_{VBS} and T_{VAS} represent the worst case data valid before and after strobe times under fast conditions.

Figure 2-5. T_{VBS} and T_{VAS} Timing Diagram



T_{VBS} = Data output valid before strobe

T_{VAS} = Data output valid after strobe

V_{REF} = V_{REF} for AGTL+ signal group

V_{high} = AGTL+ signals must achieve a DC high level of at least V_{REF} +200 mV

V_{low} = AGTL+ signals must achieve a DC low level of at least V_{REF} –200 mV

000624a

2.4.2.2.2 Delta Flight Time

The delta flight time (ΔT_{flight}) is a system dependent timing based on the maximum timing difference between the data and strobe signal flight times due to the specific PCB technology, the interface routing topology, and applicable connectors. The data signal flight time is measured from the data signal crossing a reference voltage, V_{REF}, at the output pin (of the driving agent) relative to the data signal crossing V_{REF} at the input pin (of the receiving agent). The strobe signal flight time is measured from the strobe signal crossing a reference voltage, V_{REF}, at the output pin (of the driving agent) relative to the strobe signal crossing V_{REF} at the input pin (of the receiving agent).

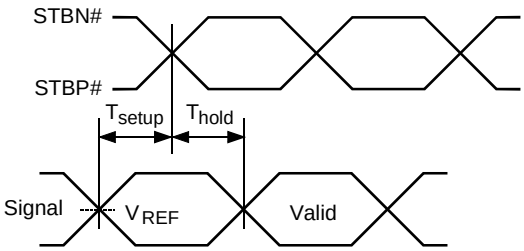
2.4.2.2.3 Receiver Setup and Hold to Strobe

The receiver setup and hold to strobe (T_{setup} and T_{hold}) is defined by the signal at the input pin (of the receiving agent) crossing a reference voltage, V_{REF}, relative to the differential strobe crossing at the input pin (of the receiving agent). T_{setup} and T_{hold} each include the internal clock skew and tester guardband.

Figure 2-6 illustrates the T_{setup} and T_{hold} timing definition, and Table 2-13 lists the T_{setup} and T_{hold} values for the source synchronous system bus signals. T_{setup} represents the worst case setup time requirement under slow conditions. T_{hold} represents the worst case hold time requirement under fast conditions.

Table 2-13 shows the source synchronous AC timing parameters under worst case conditions in a tester environment. These parameters are intended to provide a method for verifying the component's I/O timings in a real system. All timings are specified to the pin of the component at a rated load of 20Ω. The voltage reference is V_{REF}.

Figure 2-6. Source Synchronous Mode Data Setup and Hold Timings



T_{setup} = Data output valid before strobe

T_{hold} = Data output valid after strobe

V_{REF} = V_{REF} for AGTL+ signal group

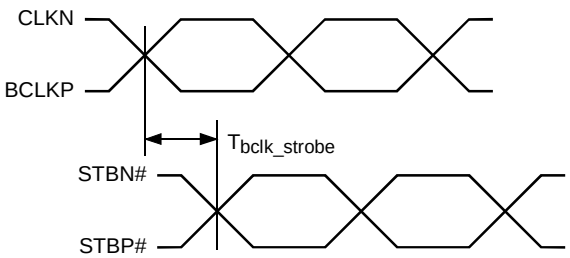
000625b

Table 2-13. AGTL+ Data Signal Group Source Synchronous AC Timing Specifications

Symbol	Parameter	Min	Unit	Figure	Notes
T_{VBS}	Data Output H → L Valid Before Strobe	1.56	ns	2-5	a
T_{VBS}	Data Output L → H Valid Before Strobe	1.28	ns	2-5	a
T_{VAS}	Data Output H → L Valid After Strobe	1.40	ns	2-5	a
T_{VAS}	Data Output L → H Valid After Strobe	1.60	ns	2-5	a
T_{setup}	Data Input Setup Time Before Strobe	0.63	ns	2-6	
T_{hold}	Data Input Hold Time After Strobe	0.59	ns	2-6	
T_{bclk_strobe}	Clock to Strobe Delay Time	T_{CO_MIN} + (1/4*T_{period})	ns	2-7	b, c

a. Valid timings for these signals are specified into an idealized 20-ohm resistor to VCTERM. Data/strobe offset is 1.875 ns (one quarter clock cycle) at the latch output.
b. The strobe signals are generated from the bus clock signals.
c. These Tco,min and Tco,max specifications are for data signals and are found in Table 2-11.

Figure 2-7. Bus Clock to Strobe Delay Timing



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2.4.3 AC Specifications for Clock, Test Access Port, and System Management Bus

Table 2-14 through Table 2-16 list the AC specifications for the Itanium processor's clock, test access port, and system management bus (timing diagrams begin with Figure 2-8). The Itanium processor uses a differential HSTL clocking scheme with a frequency of 133 MHz. The test access port (TAP) interface is used for system level debug and operates at speeds up to 16 MHz. The TAP signals' AC specifications at the processor are listed in Table 2-16. The system management bus (SMBus) is a standard I2C interface which supports operation of up to 100 kHz.

Table 2-14. System Bus Clock Differential HSTL AC Specifications

Symbol	Parameter	Min	Typical	Max	Unit	Figure	Notes
T_{period}	BCLK Period	7.5		7.65	ns	2-8	a, b
f_{BCLK}	BCLK Frequency	130.72		133.33	MHz		c
$T_{jitter,i}$	BCLK Input Jitter			100	ps	2-8	d, e, f, g
T_{high}	BCLK High Time	3.375		4.125	ns	2-8	
T_{low}	BCLK Low Time	3.375		4.125	ns	2-8	
T_{rise}	BCLK Rise Time	0.6		1.2	ns	2-8	20–80%
T_{fall}	BCLK Fall Time	0.6		1.2	ns	2-8	20–80%
V_{PP}	Minimum Input Swing	600			mV	2-8	h

a. The internal core clock frequency is derived from the bus clock.
b. The period specified here is the average period. A given period may vary from this specification as governed by the Input Jitter specification ($T_{jitter,i}$).
c. Data is transferred at twice this frequency in source synchronous mode.
d. Input clock jitter is measured at the cross point of the rising edge of BCLKP and the falling edge of BCLKN. The specification corresponds to the cycle-to-cycle (peak to peak) jitter (i.e. the Nth cycle to the N+1th cycle at any bus cycle N).
e. The measurement should be done at the location closest to the corresponding pins of the microprocessor cartridge.
f. The system clock driver's close loop jitter bandwidth must be less than 500 KHz (at -20 dB) and preferably less than 100 KHz. The bandwidth is defined as the clock driver's output frequency-attenuation plot measured at the -20dB attenuation point.
g. The measurement should be performed with a dedicated jitter measurement instrument (examples: Wavecrest Corp.'s DTS system or the Amherst's M1 system). Measurements performed with an oscilloscope using the infinite persistence method may yield poor results.
h. V_{PPmin} is defined as the minimum input differential voltage which will cause no increase in the clock receiver timing.

Figure 2-8. System Clock Waveform

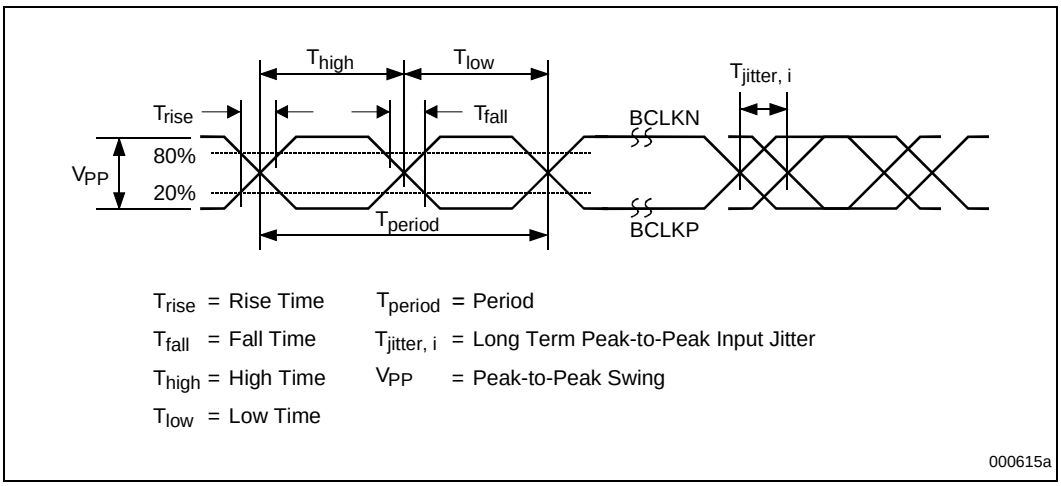


Table 2-15. TAP Signal AC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
T_{CO}	Clock to Output delay	1.0	10.0	ns	a
TDO_{delay}	TDO on/off delay		25.0	ns	a
T_{setup}	Input setup time for TDI, TMS, and TRST#	5.0		ns	b
T_{hold}	Input hold time for TDI, TMS, and TRST#	5.0		ns	b

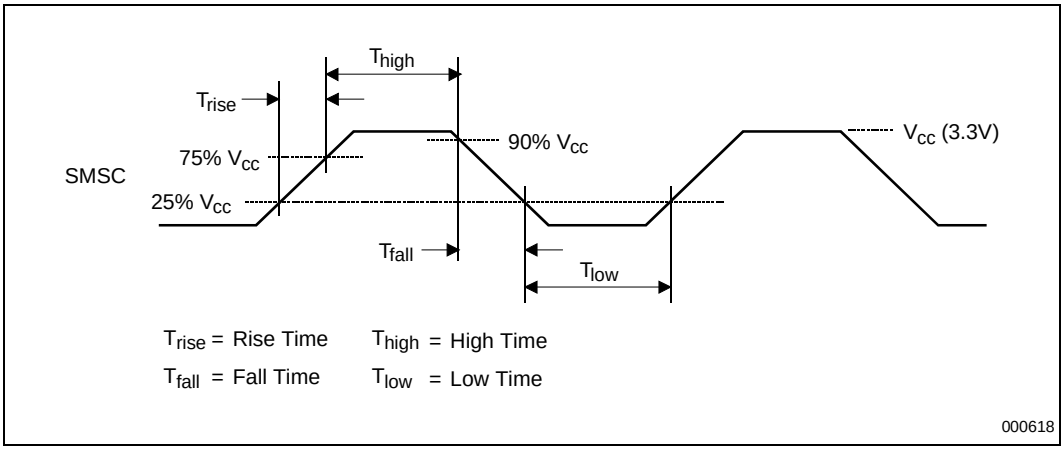
a. Referenced to TCK falling edge.
b. Referenced to TCK rising edge.

Table 2-16. SMBus Signal AC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
f_{SMSC}	SMSC Clock Frequency		100	kHz	
T_{SMSC}	SMSC Clock Period	10		µs	
T_{high}	SMSC Clock High Time	4.0		µs	a
T_{low}	SMSC Clock Low Time	4.7		µs	a
T_{rise}	SMSC Clock Rise Time		1.0	µs	a
T_{fall}	SMSC Clock Fall Time		0.3	µs	a
T_{valid}	SMBus Output Valid Delay		1.0	µs	
T_{setup}	SMBus Input Setup Time	250		ns	
T_{hold}	SMBus Input Hold Time	0		ns	
T_{free}	Bus Free Time	4.7		µs	b

a. Please refer to Figure 2-9.
b. Bus Free Time is the minimum time allowed between request cycles.

Figure 2-9. SMSC Clock Waveform



2.4.4 Maximum Ratings

Table 2-17 contains Intel Itanium processor stress ratings. Functional operation at the absolute maximum and minimum is neither implied nor guaranteed. The processor should not receive a clock while subjected to these conditions. Functional operating conditions are given in the AC and DC tables. Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the processor contains protective circuitry to resist damage from static electric discharge, one should always take precautions to avoid high static voltages or electric fields.

Table 2-17. Intel® Itanium™ Processor Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
$T_{storage}$	Processor Storage Temperature	5.0	45.0	°C	a
$T_{shipping}$	Processor Shipping Temperature	–40.0	75.0	°C	a
$VCC_{processor}$	Any $VCC_{processor}$ voltage with respect to GND	–0.35	2.1	V	b
VCC_{cache}	Any VCC_{cache} voltage with respect to GND	–0.5	2.8	V	b
VREF	Any VREF voltage with respect to GND	–0.3	1.046 (2/3$VCTERM_{max}$)	V	
3.3V	Any 3.3V supply voltage with respect to GND	–0.3	5.5	V	
$VCC_{processor}$ –VCC_{cache}	Cache supply voltage with respect to processor supply voltage	– 1.7	2.23	V	c

a. The PAC418 package and integrated vapor chamber technology has been designed and tested to withstand up to 50 freeze/thaw cycles.
b. Operating voltage is the voltage to which the component is designed to operate. See Table 2-6 throughTable 2-9 inclusive.
c. This parameter specifies that the processor will not be immediately damaged by either supply being disabled.

2.5 Power Pod Connector Signals

Power delivery for the Intel Itanium processor cartridge is from a DC-DC converter called the “power pod”. The power pod consists of a DC-DC converter and a semi-flexible connector which delivers the voltage to the cartridge.

Table 2-18 lists all of the signals which are part of the Intel Itanium processor cartridge power pod connector.

Table 2-18. Intel® Itanium™ Processor Power Pod Connector Signals

Group Name	Signals
Power Pod Connector	OUTEN, PROCPRES#, PPODGD#, SenseCacheVCC, SenseCacheVSS, SenseProcVCC, SenseProcVSS, VCC_PROCESSOR, VCC_CACHE, VID_PROCESSOR[3:0], VID_CACHE[3:0], VSS_PROCESSOR

The operating voltage of the processor core and of the L3 cache die differ from each other. Both of these voltages, $VCC_{processor}$ and VCC_{cache}, are supplied by the power pod through the power tab connector on the Intel Itanium processor PAC418 cartridge. Figure 2-10 and Figure 2-11 are top and bottom views of the power tab connector, respectively. Processor ground connection, $VSS_{processor}$, is provided on the power tab connector as well.

Figure 2-10. Intel® Itanium™ Processor Power Tab Connection (Top View)

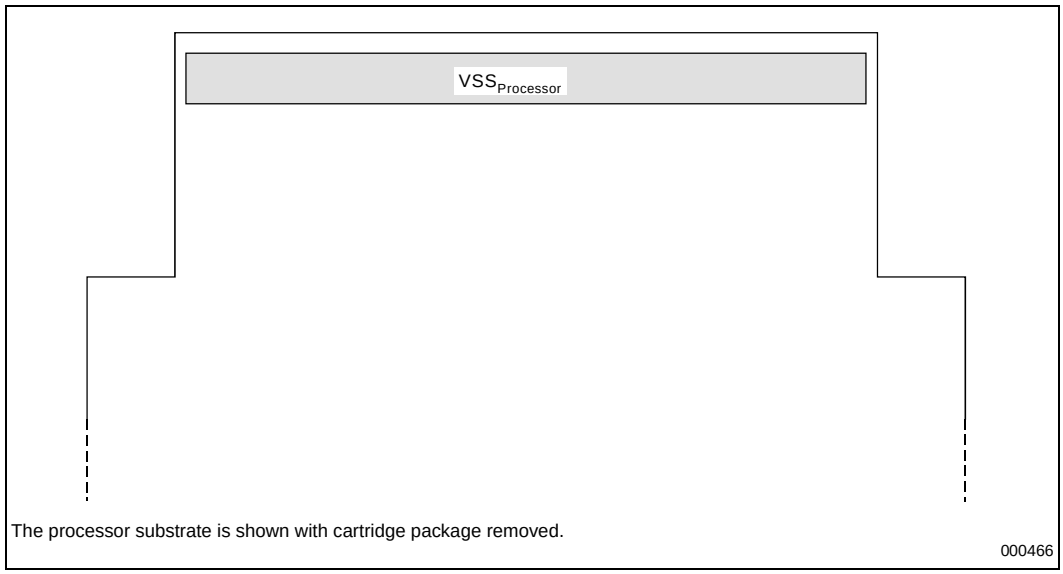
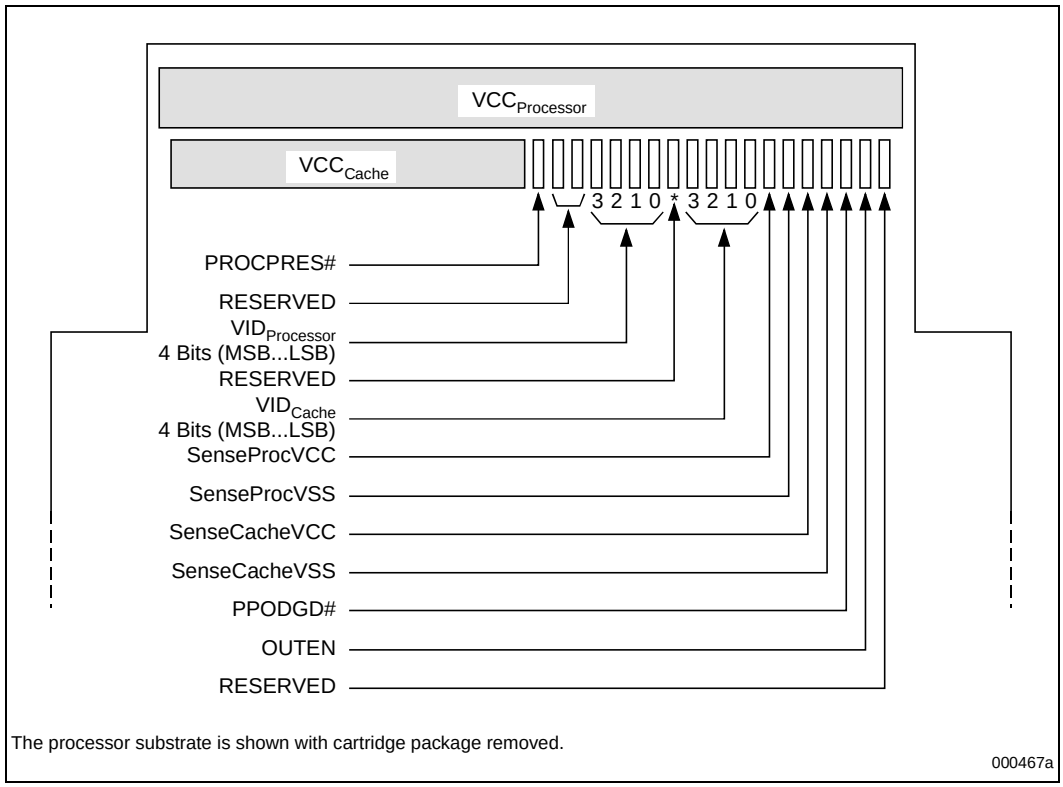


Figure 2-11. Intel® Itanium™ Processor Power Tab Connection (Bottom View)



The Intel Itanium processor cartridge power pod connector contains VID voltage identification signals which program the DC-DC converter in the power pod to provide voltages which are required by various components in the cartridge. The VID signals are needed to support voltage specification variations on the Intel Itanium processor cartridge.

The VID signals are static and are either an open circuit or a short to ground. The combination of open and short circuits defines the voltages required by the Intel Itanium processor cartridge.

Warning: If the power pod cannot supply the voltages requested by the components in the Intel Itanium processor cartridge, then it must disable itself.

The voltages specified by the various VID signal combinations for the processor core and cache core are listed in Table 2-19 and Table 2-20, respectively. A '1' in this table refers to an open circuit and a '0' refers to a short to ground. The VID settings and processor and cache core voltages are recorded in the EEPROM and can be accessed by the SMBus (see Chapter 6 for more information).

Table 2-19. Processor Core Voltage Identification Code

VID_PROCESSOR[3:0]				$VCC_{processor}$ (VDC)
VID_PROCESSOR3	VID_PROCESSOR2	VID_PROCESSOR1	VID_PROCESSOR0	
1	1	1	1	Output off
1	1	1	0	1.250
1	1	0	1	1.275
1	1	0	0	1.300
1	0	1	1	1.325
1	0	1	0	1.350
1	0	0	1	1.375
1	0	0	0	1.400
0	1	1	1	1.425
0	1	1	0	1.450
0	1	0	1	1.475
0	1	0	0	1.500
0	0	1	1	1.525
0	0	1	0	1.550
0	0	0	1	1.575
0	0	0	0	1.600

Table 2-20. Cache Voltage Identification Code

VID_CACHE[3:0]				VCC_{cache} (VDC)
VID_CACHE3	VID_CACHE2	VID_CACHE1	VID_CACHE0	
1	1	1	1	Output off
1	0	0	1	1.650
1	0	0	0	1.700
0	1	1	1	1.750
0	1	1	0	1.800
0	1	0	1	1.850
0	1	0	0	1.900
0	0	1	1	1.950

Table 2-20. Cache Voltage Identification Code (Cont'd)

VID_CACHE[3:0]				VCC_{cache} (VDC)
VID_CACHE3	VID_CACHE2	VID_CACHE1	VID_CACHE0	
0	0	1	0	2.000
0	0	0	1	2.050
0	0	0	0	2.100

Table 2-21 shows the slew rate requirements for both outputs of the power pod.

Table 2-21. Power Pod Slew Rate Requirements

Output	Peak Slew Rate at the Power Pod Connector
$VCC_{processor}$	400 A/µs
VCC_{cache}	100 A/µs

2.6 Intel® Itanium™ Processor System Bus Clock and Processor Clocking

The BCLKN and BCLKP inputs control the operating frequency of the Intel Itanium processor system bus interface. All Intel Itanium processor system bus timing parameters are specified with respect to the falling edge of BCLKN and rising edge of BCLKP. The Intel Itanium processor core to bus ratio must be configured during system reset by using the A20M#, IGNNE#, and LINT[1:0] pins (See Table 2-22). The value on these pins during the system reset sequence determines the multiplier that the phase lock loop (PLL) will use for the internal core clock. See Figure 2-13 for the timing relationship between the system bus multiplier signals, system reset signal and normal processor operation.

Because the signals A20M#, IGNNE#, and LINT[1:0] pins have different uses after a system reset is complete, these signals must be multiplexed for configuration during reset and for normal use after reset. The circuit in Figure 2-12 suggested one way to use the system reset signal and a multiplexer to share these configuration signals. Note that this system reset signal must be driven 2 clock cycles longer than the processor reset signal to meet the timing requirements in Figure 2-13. The level translators after the multiplexer translates 3.3V output levels to the correct AGTL+ levels (1.5V) required by the Intel Itanium processors.

Table 2-22 lists the system bus ratio defined for the Intel Itanium processor family.

Figure 2-12. Example Schematic for System Bus Multiplier Pin Sharing

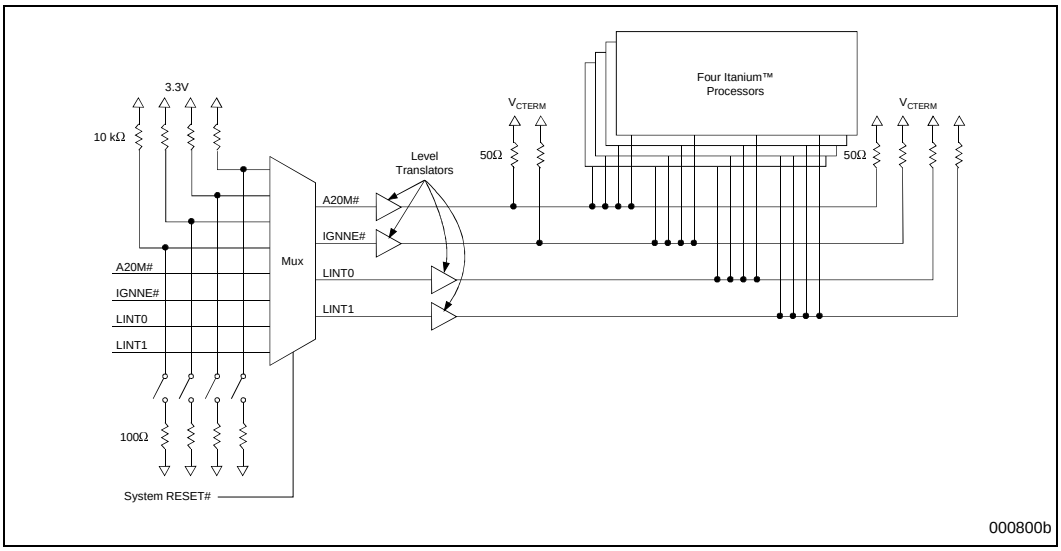


Table 2-22. Intel® Itanium™ Processor System Bus Ratios Supported

Ratio of Bus Frequency to Core Frequency	LINT1	LINT0	IGNNE#	A20M#
2/11	0(L)	0(L)	0(H)	0(H)
2/12	0(L)	1(H)	1(L)	1(L)
Reserved	All other combinations			

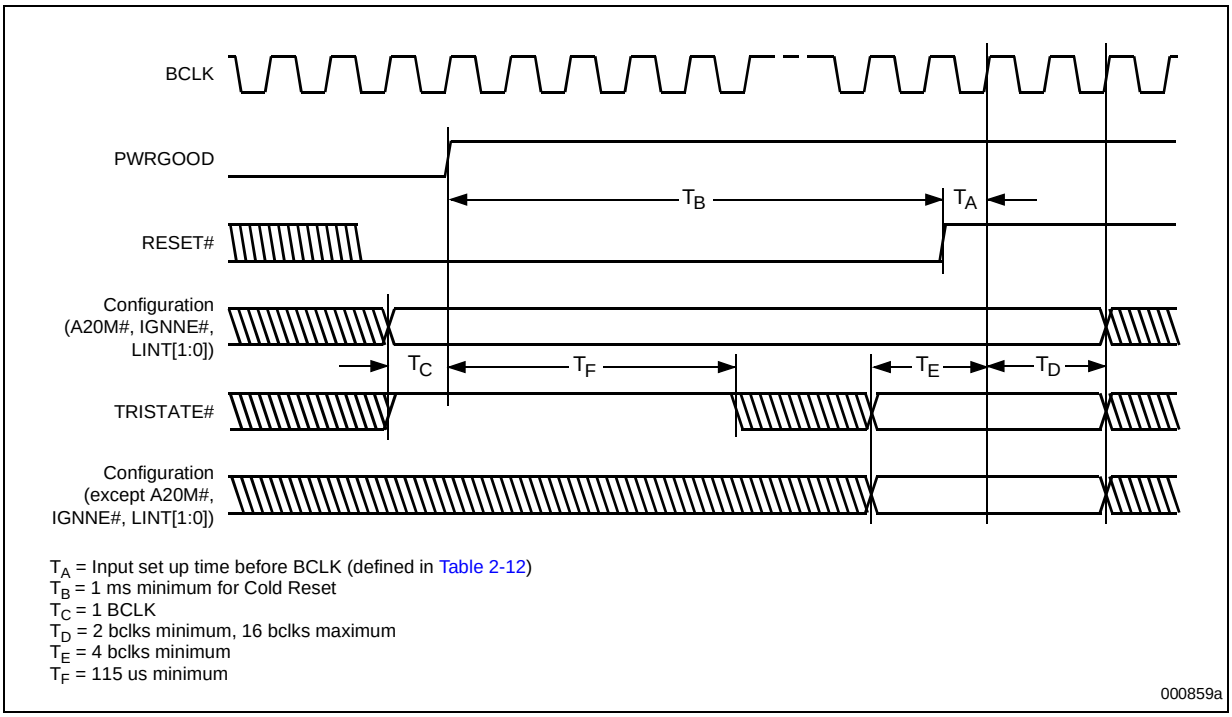
The Itanium processor core to bus ratio is configured during system reset by using the A20M#, IGNNE# and LINT[1:0] pins. These bus ratio configuration pins are required be to be stable and valid during the duration of the reset sequence as defined below.

Cold Reset Sequence:

- The bus ratio configuration pins (A20M#, IGNNE#, LINT1, and LINT0) must be stable and valid at least 1 BCLK before the assertion edge of PWRGOOD.
- TRISTATE# must be disabled 1 BCLK before the assertion of PWRGOOD and held disabled for at least 115 microseconds.
- RESET# must be asserted before PWRGOOD is asserted.
- The duration from the assertion of PWRGOOD to the deassertion of RESET# must be 1 millisecond minimum.
- After RESET# is deasserted, the bus ratio configuration pins must remain valid for 2 BCLKs (minimum) to 16 BCLKs (maximum).
- BCLK is shown as a time reference to the BCLK period. It is not a requirement that this is BCLKN or BCLKP signal.

Figure 2-13 outlines the timing relationship between the bus ratio configuration pins, RESET# and PWRGOOD for cold reset.

Figure 2-13. System Bus Reset and Configuration Timings for Cold Reset

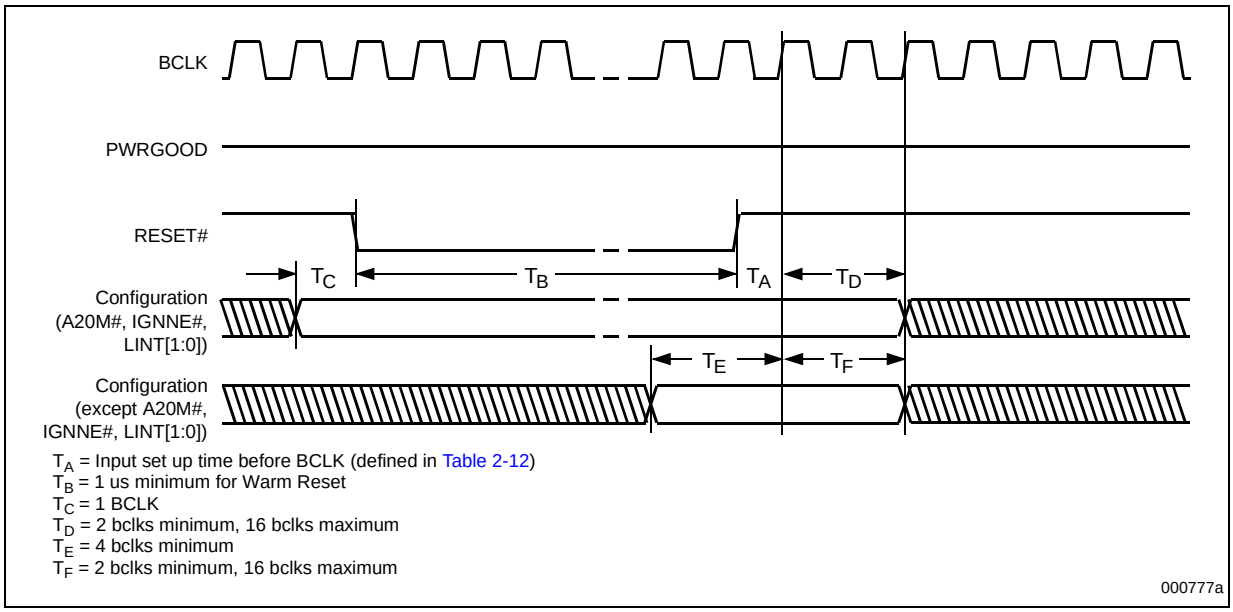


Warm Reset Sequence:

- PWRGOOD remains high throughout the entire sequence as power is already available and stable to the processor.
- The bus ratio configuration pins (A20M#, IGNNE#, LINT1, and LINT0) must be stable and valid at least 1 BCLK before the assertion edge of RESET#.
- The duration from the assertion of RESET# to the deassertion of RESET# must be 1 microsecond minimum.
- After RESET# is deasserted, the bus clock ratio configuration pins must remain valid for 2 BCLKs (minimum) to 16 BCLKs (maximum).
- BCLK is shown as a time reference to the BCLK period. It is not a requirement that this is BCLKN or BCLKP signal.

Figure 2-14 outlines the timing relationship between the bus ratio configuration pins, RESET# and PWRGOOD for warm reset

Figure 2-14. System Bus Reset and Configuration Timings for Warm Reset



2.7 Signal Quality and Noise Margin

The Intel Itanium processor has overshoot/undershoot requirements for system bus signals. A waveform exhibiting undershoot/overshoot is illustrated in Figure 2-15. These requirements stipulate that a signal at the output of the driver buffer and input of the receiver buffer must not exceed a maximum absolute overshoot voltage limit and a minimum absolute undershoot voltage limit. There is also a time dependent, non-linear overshoot requirement above VCTERM and an undershoot requirement below GND which is dependent on the amplitude and duration of the overshoot/undershoot. The maximum specifications for signal quality is listed in Table 2-23. Exceeding these limits may cause damage to the Intel Itanium processor.

Figure 2-15. Example Data Signal Waveform at Intel® Itanium™ Processor Receiver Pad

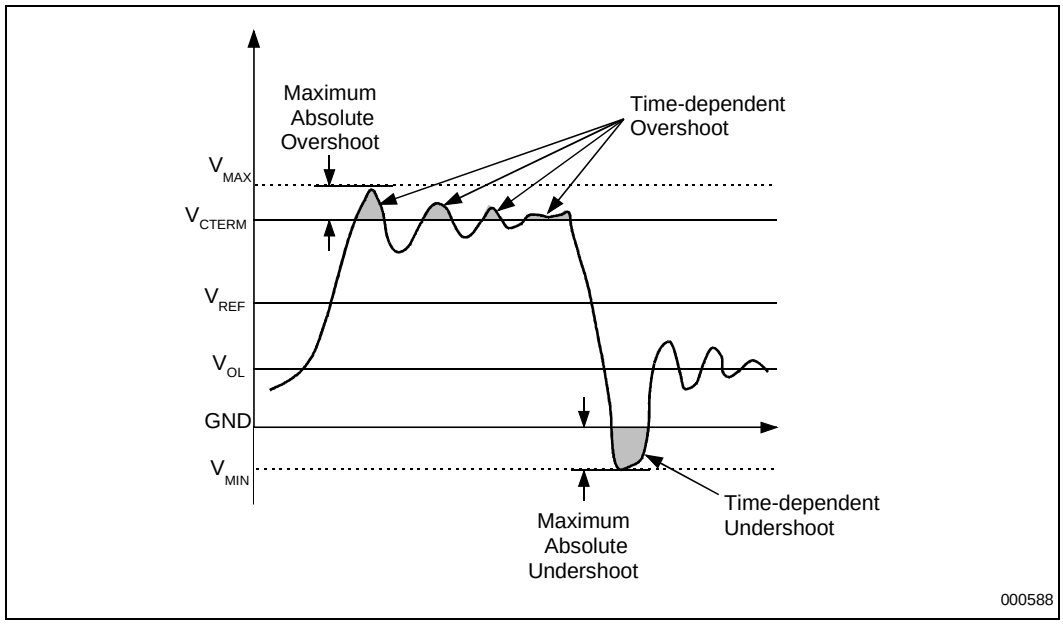


Table 2-23. Signal Quality Specifications for System Bus Signals at Intel® Itanium™ Processor Receiver Pad

Parameter	Description	Specification	Units
V_{MAX}	Maximum absolute voltage for system bus signals at the inputs of receiver buffers	2.1	V
V_{MIN}	Minimum absolute voltage for system bus signals at the inputs of receiver buffers	–0.35	V

2.8 Recommended Connections for Unused Pins

Pins that are unused in an application environment (as opposed to testing environment) should be connected to the states listed in Table 2-24. Pins that must be used in an application are stated as such and do not have a recommended state for unused connection.

Table 2-24. Connection for Unused Pins

Pins / Pin Groups	Recommended Connections	Notes
AGTL+ pins	H	b
HSTL Clock Signals	Must be used	
TAP Signals		
TCK	L	b
TRST#	H	b
TDI	H	b
TDO	H	b
TMS	H	b

Table 2-24. Connection for Unused Pins (Cont'd)

Pins / Pin Groups	Recommended Connections	Notes
PWRGOOD Signal		
PWRGOOD	Must be used	
System Management Signals		
3.3V	GND	a
SMA	N/C	
SMSC	N/C	
SMSD	N/C	
SMWP	N/C	
THRMALERT#	H	c
All Power Signals	Must be used	
Power Signals		
All Power Signals	Must be used	
LVTTL Power Pod Signals		
OUTEN	Must be used	
PPODGD#	Must be used	
Other Signals		
PROCPRES#	Must be used	
TUNER[1:0]	Must be used	
Reserved Pins		
N/C	N/C	
PD[3:0]	L	b
PU[2:0]	H	d, e

a. All 3.3V pins must be connected to either 3.3V or GND, at the same time.
b. L = GND, H = VCTERM.
c. THRMALERT# should be pulled up to 3.3V through a resistor. If the system does not supply 3.3V for system management, then this signal should be left unconnected.
d. PU1 should be pulled up through a 100 ohm resistor.
e. PU0 and PU2 should be pulled up through 1 kohm resistors.

Pinout Specifications 3

This chapter describes the Intel Itanium processor signals and the Intel Itanium processor cartridge pinout. Please note that the “N/C” pins are reserved pins and must remain unconnected. The Intel Itanium processor cartridge uses a JEDEC standard pin naming convention.

In this chapter, pin names are the actual names given to each physical pin of the processor. System bus signal names are the names associated with the functions of those pins. For those pins associated with multi functions, their pin names and system bus signal names are not necessarily identical.

Figure 3-1. Intel® Itanium™ Processor PAC418 Cartridge Pin Locations (Top View)

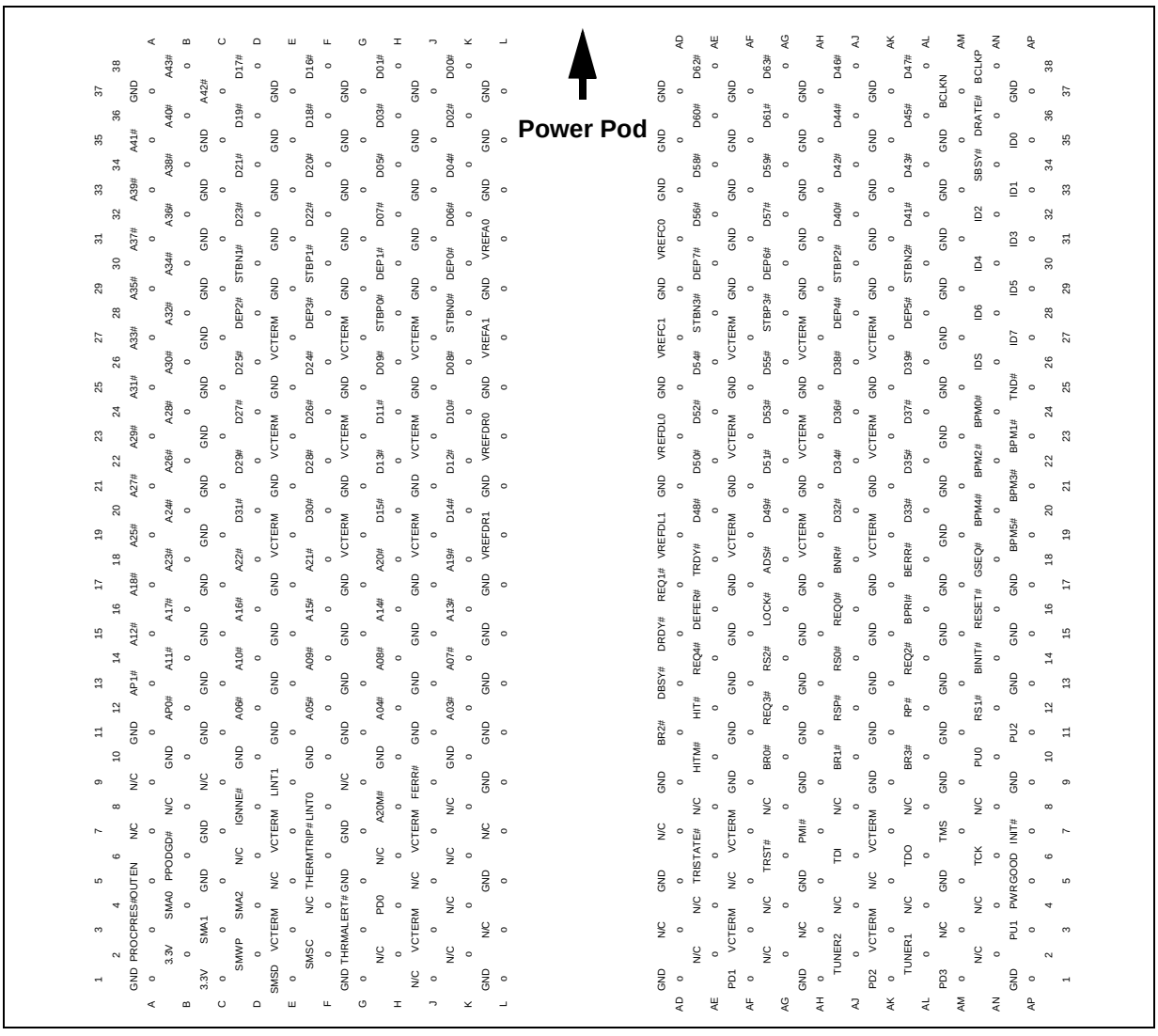


Table 3-1. Pin/Signal Information Sorted by Pin Name

Pin Name	System Bus Signal Name	Pin Location	Input/Output
3.3V		C01	IN
3.3V		B02	IN
A03#	AA03#/EXF0#/DPS#	K12	IN/OUT
A04#	AA04#/EXF1#/DEN#	H12	IN/OUT
A05#	AA05#/EXF2#/OWN#	F12	IN/OUT
A06#	AA06#/EXF3#/FCL#/SPLCK#	D12	IN/OUT
A07#	AA07#/EXF4#	K14	IN/OUT
A08#	AA08#/BE0#	H14	IN/OUT
A09#	AA09#/BE1#	F14	IN/OUT
A10#	AA10#/BE2#	D14	IN/OUT
A11#	AA11#/BE3#	B14	IN/OUT
A12#	AA12#/BE4#	A15	IN/OUT
A13#	AA13#/BE5#	K16	IN/OUT
A14#	AA14#/BE6#	H16	IN/OUT
A15#	AA15#/BE7#	F16	IN/OUT
A16#	AA16#/DID0#	D16	IN/OUT
A17#	AA17#/DID1#	B16	IN/OUT
A18#	AA18#/DID2#	A17	IN/OUT
A19#	AA19#/DID3#	K18	IN/OUT
A20#	AA20#/DID4#	H18	IN/OUT
A20M#	A20M#	H08	IN
A21#	AA21#/DID5#	F18	IN/OUT
A22#	AA22#/DID6#	D18	IN/OUT
A23#	AA23#/DID7#	B18	IN/OUT
A24#	AA24#/ATTR0#	B20	IN/OUT
A25#	AA25#/ATTR1#	A19	IN/OUT
A26#	AA26#/ATTR2#	B22	IN/OUT
A27#	AA27#/ATTR3#	A21	IN/OUT
A28#	AA28#/ATTR4#	B24	IN/OUT
A29#	AA29#/ATTR5#	A23	IN/OUT
A30#	AA30#/ATTR6#	B26	IN/OUT
A31#	AA31#/ATTR7#	A25	IN/OUT
A32#	AA32#/AB32#	B28	IN/OUT
A33#	AA33#/AB33#	A27	IN/OUT
A34#	AA34#/AB34#	B30	IN/OUT
A35#	AA35#/AB35#	A29	IN/OUT
A36#	AA36#/AB36#	B32	IN/OUT
A37#	AA37#/AB37#	A31	IN/OUT
A38#	AA38#/AB38#	B34	IN/OUT
A39#	AA39#/AB39#	A33	IN/OUT
A40#	AA40#/AB40#	B36	IN/OUT
A41#	AA41#/AB41#	A35	IN/OUT
A42#	AA42#/AB42#	C37	IN/OUT
A43#	AA43#/AB43#	B38	IN/OUT

Table 3-1. Pin/Signal Information Sorted by Pin Name (Cont'd)

Pin Name	System Bus Signal Name	Pin Location	Input/Output
ADS#	ADS#	AG18	IN/OUT
AP0#	AP0#	B12	IN/OUT
AP1#	AP1#	A13	IN/OUT
BCLKN	BCLKN	AM37	IN
BCLKP	BCLKP	AN38	IN
BERR#	BERR#	AL18	IN/OUT
BINIT#	BINIT#	AN14	IN/OUT
BNR#	BNR#	AJ18	IN/OUT
BPM0#	BPM0#	AN24	IN/OUT
BPM1#	BPM1#	AP23	IN/OUT
BPM2#	BPM2#	AN22	IN/OUT
BPM3#	BPM3#	AP21	IN/OUT
BPM4#	BPM4#	AN20	IN/OUT
BPM5#	BPM5#	AP19	IN/OUT
BPRI#	BPRI#	AL16	IN
BR0#	BREQ0#	AG10	IN/OUT
BR1#	BREQ1#	AJ10	IN
BR2#	BREQ2#	AD11	IN
BR3#	BREQ3#	AL10	IN
D00#	D00#	K38	IN/OUT
D01#	D01#	H38	IN/OUT
D02#	D02#	K36	IN/OUT
D03#	D03#	H36	IN/OUT
D04#	D04#	K34	IN/OUT
D05#	D05#	H34	IN/OUT
D06#	D06#	K32	IN/OUT
D07#	D07#	H32	IN/OUT
D08#	D08#	K26	IN/OUT
D09#	D09#	H26	IN/OUT
D10#	D10#	K24	IN/OUT
D11#	D11#	H24	IN/OUT
D12#	D12#	K22	IN/OUT
D13#	D13#	H22	IN/OUT
D14#	D14#	K20	IN/OUT
D15#	D15#	H20	IN/OUT
D16#	D16#	F38	IN/OUT
D17#	D17#	D38	IN/OUT
D18#	D18#	F36	IN/OUT
D19#	D19#	D36	IN/OUT
D20#	D20#	F34	IN/OUT
D21#	D21#	D34	IN/OUT
D22#	D22#	F32	IN/OUT
D23#	D23#	D32	IN/OUT
D24#	D24#	F26	IN/OUT
D25#	D25#	D26	IN/OUT

Table 3-1. Pin/Signal Information Sorted by Pin Name (Cont'd)

Pin Name	System Bus Signal Name	Pin Location	Input/Output
D26#	D26#	F24	IN/OUT
D27#	D27#	D24	IN/OUT
D28#	D28#	F22	IN/OUT
D29#	D29#	D22	IN/OUT
D30#	D30#	F20	IN/OUT
D31#	D31#	D20	IN/OUT
D32#	D32#	AJ20	IN/OUT
D33#	D33#	AL20	IN/OUT
D34#	D34#	AJ22	IN/OUT
D35#	D35#	AL22	IN/OUT
D36#	D36#	AJ24	IN/OUT
D37#	D37#	AL24	IN/OUT
D38#	D38#	AJ26	IN/OUT
D39#	D39#	AL26	IN/OUT
D40#	D40#	AJ32	IN/OUT
D41#	D41#	AL32	IN/OUT
D42#	D42#	AJ34	IN/OUT
D43#	D43#	AL34	IN/OUT
D44#	D44#	AJ36	IN/OUT
D45#	D45#	AL36	IN/OUT
D46#	D46#	AJ38	IN/OUT
D47#	D47#	AL38	IN/OUT
D48#	D48#	AE20	IN/OUT
D49#	D49#	AG20	IN/OUT
D50#	D50#	AE22	IN/OUT
D51#	D51#	AG22	IN/OUT
D52#	D52#	AE24	IN/OUT
D53#	D53#	AG24	IN/OUT
D54#	D54#	AE26	IN/OUT
D55#	D55#	AG26	IN/OUT
D56#	D56#	AE32	IN/OUT
D57#	D57#	AG32	IN/OUT
D58#	D58#	AE34	IN/OUT
D59#	D59#	AG34	IN/OUT
D60#	D60#	AE36	IN/OUT
D61#	D61#	AG36	IN/OUT
D62#	D62#	AE38	IN/OUT
D63#	D63#	AG38	IN/OUT
DBSY#	DBSY#	AD13	IN/OUT
DEFER#	DEFER#	AE16	IN
DEP0#	DEP0#	K30	IN/OUT
DEP1#	DEP1#	H30	IN/OUT
DEP2#	DEP2#	D28	IN/OUT
DEP3#	DEP3#	F28	IN/OUT
DEP4#	DEP4#	AJ28	IN/OUT

Table 3-1. Pin/Signal Information Sorted by Pin Name (Cont'd)

Pin Name	System Bus Signal Name	Pin Location	Input/Output
DEP5#	DEP5#	AL28	IN/OUT
DEP6#	DEP6#	AG30	IN/OUT
DEP7#	DEP7#	AE30	IN/OUT
DRATE#	DRATE#	AN36	IN
DRDY#	DRDY#	AD15	IN/OUT
FERR#	FERR#	J09	OUT
GND	GND	A11	IN
GND	GND	B10	IN
GND	GND	A01	IN
GND	GND	C05	IN
GND	GND	C07	IN
GND	GND	C11	IN
GND	GND	C13	IN
GND	GND	C15	IN
GND	GND	C17	IN
GND	GND	C19	IN
GND	GND	C21	IN
GND	GND	C23	IN
GND	GND	C25	IN
GND	GND	C27	IN
GND	GND	C29	IN
GND	GND	C31	IN
GND	GND	C33	IN
GND	GND	C35	IN
GND	GND	A37	IN
GND	GND	D10	IN
GND	GND	E11	IN
GND	GND	E13	IN
GND	GND	E15	IN
GND	GND	E17	IN
GND	GND	E21	IN
GND	GND	E25	IN
GND	GND	E29	IN
GND	GND	E31	IN
GND	GND	E33	IN
GND	GND	E35	IN
GND	GND	E37	IN
GND	GND	F10	IN
GND	GND	G01	IN
GND	GND	G05	IN
GND	GND	G07	IN
GND	GND	G11	IN
GND	GND	G13	IN
GND	GND	G15	IN
GND	GND	G17	IN

Table 3-1. Pin/Signal Information Sorted by Pin Name (Cont'd)

Pin Name	System Bus Signal Name	Pin Location	Input/Output
GND	GND	G21	IN
GND	GND	G25	IN
GND	GND	G29	IN
GND	GND	G31	IN
GND	GND	G33	IN
GND	GND	G35	IN
GND	GND	G37	IN
GND	GND	H10	IN
GND	GND	J11	IN
GND	GND	J13	IN
GND	GND	J15	IN
GND	GND	J17	IN
GND	GND	J21	IN
GND	GND	J25	IN
GND	GND	J29	IN
GND	GND	J31	IN
GND	GND	J33	IN
GND	GND	J35	IN
GND	GND	J37	IN
GND	GND	K10	IN
GND	GND	L01	IN
GND	GND	L05	IN
GND	GND	L09	IN
GND	GND	L11	IN
GND	GND	L13	IN
GND	GND	L15	IN
GND	GND	L17	IN
GND	GND	L21	IN
GND	GND	L25	IN
GND	GND	L29	IN
GND	GND	L33	IN
GND	GND	L35	IN
GND	GND	L37	IN
GND	GND	AD01	IN
GND	GND	AD05	IN
GND	GND	AD09	IN
GND	GND	AD21	IN
GND	GND	AD25	IN
GND	GND	AD29	IN
GND	GND	AD33	IN
GND	GND	AD35	IN
GND	GND	AD37	IN
GND	GND	AF09	IN
GND	GND	AF11	IN
GND	GND	AF13	IN

Table 3-1. Pin/Signal Information Sorted by Pin Name (Cont'd)

Pin Name	System Bus Signal Name	Pin Location	Input/Output
GND	GND	AF15	IN
GND	GND	AF17	IN
GND	GND	AF21	IN
GND	GND	AF25	IN
GND	GND	AF29	IN
GND	GND	AF31	IN
GND	GND	AF33	IN
GND	GND	AF35	IN
GND	GND	AF37	IN
GND	GND	AH01	IN
GND	GND	AH05	IN
GND	GND	AH09	IN
GND	GND	AH11	IN
GND	GND	AH13	IN
GND	GND	AH15	IN
GND	GND	AH17	IN
GND	GND	AH21	IN
GND	GND	AH25	IN
GND	GND	AH29	IN
GND	GND	AH31	IN
GND	GND	AH33	IN
GND	GND	AH35	IN
GND	GND	AH37	IN
GND	GND	AK09	IN
GND	GND	AK11	IN
GND	GND	AK13	IN
GND	GND	AK15	IN
GND	GND	AK17	IN
GND	GND	AK21	IN
GND	GND	AK25	IN
GND	GND	AK29	IN
GND	GND	AK31	IN
GND	GND	AK33	IN
GND	GND	AK35	IN
GND	GND	AK37	IN
GND	GND	AP01	IN
GND	GND	AM05	IN
GND	GND	AM09	IN
GND	GND	AM11	IN
GND	GND	AM13	IN
GND	GND	AM15	IN
GND	GND	AM17	IN
GND	GND	AM19	IN
GND	GND	AM21	IN
GND	GND	AM23	IN

Table 3-1. Pin/Signal Information Sorted by Pin Name (Cont'd)

Pin Name	System Bus Signal Name	Pin Location	Input/Output
GND	GND	AM25	IN
GND	GND	AM27	IN
GND	GND	AM29	IN
GND	GND	AM31	IN
GND	GND	AM33	IN
GND	GND	AM35	IN
GND	GND	AP37	IN
GND	GND	AP09	IN
GND	GND	AP13	IN
GND	GND	AP15	IN
GND	GND	AP17	IN
GSEQ#	GSEQ#	AN18	IN
HIT#	HIT#	AE12	IN/OUT
HITM#	HITM#	AE10	IN/OUT
ID0#	IDA0#/IP0#	AP35	IN
ID1#	IDA1#/IP1#	AP33	IN
ID2#	IDA2#/DHIT#	AN32	IN
ID3#	IDA3#/IDB3#	AP31	IN
ID4#	IDA4#/IDB4#	AN30	IN
ID5#	IDA5#/IDB5#	AP29	IN
ID6#	IDA6#/IDB6#	AN28	IN
ID7#	IDA7#/IDB7#	AP27	IN
IDS#	IDS#	AN26	IN
IGNNE#	IGNNE#	D08	IN
INIT#	INIT#	AP07	IN
LINT0	INT	F08	IN
LINT1	NMI	E09	IN
LOCK#	LOCK#	AG16	IN/OUT
N/C		A07	
N/C		A09	
N/C		AM03	
N/C		AD03	
N/C		AE02	
N/C		AF05	
N/C		AG02	
N/C		AH03	
N/C		J05	
N/C		F04	
N/C		AN02	
N/C		B08	
N/C		C09	
N/C		D06	
N/C		E05	
N/C		G09	
N/C		H02	

Table 3-1. Pin/Signal Information Sorted by Pin Name (Cont'd)

Pin Name	System Bus Signal Name	Pin Location	Input/Output
N/C		H06	
N/C		J01	
N/C		K02	
N/C		K04	
N/C		K06	
N/C		K08	
N/C		L03	
N/C		L07	
N/C		AD07	
N/C		AE04	
N/C		AE08	
N/C		AG04	
N/C		AG08	
N/C		AJ04	
N/C		AJ08	
N/C		AK05	
N/C		AL04	
N/C		AL08	
N/C		AN04	
N/C		AN08	
OUTEN	OUTEN	A05	IN
PD0		H04	
PD1		AF01	
PD2		AK01	
PD3		AM01	
PMI#	PMI#	AH07	IN
PPODGD#	PPODGD#	B06	OUT
PROCPRES#	CPUPRES#	A03	OUT
PU0		AN10	
PU1		AP03	
PU2		AP11	
PWRGOOD	PWRGOOD	AP05	IN
REQ0#	REQA0#/LEN0#	AJ16	IN/OUT
REQ1#	WSNP#, D/C#/LEN1#	AD17	IN/OUT
REQ2#	REQA2#/ REQB2#	AL14	IN/OUT
REQ3#	ASZ0#/DSZ0#	AG12	IN/OUT
REQ4#	ASZ1#/DSZ1#	AE14	IN/OUT
RESET#	RESET#	AN16	IN
RP#	RP#	AL12	IN/OUT
RS0#	RS0#	AJ14	IN
RS1#	RS1#	AN12	IN
RS2#	RS2#	AG14	IN
RSP#	RSP#	AJ12	IN
SBSY#	SBSY#	AN34	IN/OUT
SMA0	SMA0	B04	IN

Table 3-1. Pin/Signal Information Sorted by Pin Name (Cont'd)

Pin Name	System Bus Signal Name	Pin Location	Input/Output
SMA1	SMA1	C03	IN
SMA2	SMA2	D04	IN
SMSC	SMSC	F02	IN
SMSD	SMSD	E01	IN/OUT
SMWP	SMWP	D02	IN
STBN0#	STBN0#	K28	IN/OUT
STBN1#	STBN1#	D30	IN/OUT
STBN2#	STBN2#	AL30	IN/OUT
STBN3#	STBN3#	AE28	IN/OUT
STBP0#	STBP0#	H28	IN/OUT
STBP1#	STBP1#	F30	IN/OUT
STBP2#	STBP2#	AJ30	IN/OUT
STBP3#	STBP3#	AG28	IN/OUT
TCK	TCK	AN06	IN
TDI	TDI	AJ06	IN
TDO	TDO	AL06	OUT
THERMTRIP#	THERMTRIP#	F06	OUT
THRMALERT#	THRMALERT#	G03	OUT
TMS	TMS	AM07	IN
TND#	TND#	AP25	IN/OUT
TRDY#	TRDY#	AE18	IN
TRISTATE#	TRISTATE#	AE06	IN
TRST#	TRST#	AG06	IN
TUNER1		AL02	IN
TUNER2		AJ02	IN
VCTERM	VCTERM	E03	IN
VCTERM	VCTERM	E07	IN
VCTERM	VCTERM	E19	IN
VCTERM	VCTERM	E23	IN
VCTERM	VCTERM	E27	IN
VCTERM	VCTERM	G19	IN
VCTERM	VCTERM	G23	IN
VCTERM	VCTERM	G27	IN
VCTERM	VCTERM	J03	IN
VCTERM	VCTERM	J07	IN
VCTERM	VCTERM	J19	IN
VCTERM	VCTERM	J23	IN
VCTERM	VCTERM	J27	IN
VCTERM	VCTERM	AF03	IN
VCTERM	VCTERM	AF07	IN
VCTERM	VCTERM	AF19	IN
VCTERM	VCTERM	AF23	IN
VCTERM	VCTERM	AF27	IN
VCTERM	VCTERM	AH19	IN
VCTERM	VCTERM	AH23	IN

Table 3-1. Pin/Signal Information Sorted by Pin Name (Cont'd)

Pin Name	System Bus Signal Name	Pin Location	Input/Output
VCTERM	VCTERM	AH27	IN
VCTERM	VCTERM	AK03	IN
VCTERM	VCTERM	AK07	IN
VCTERM	VCTERM	AK19	IN
VCTERM	VCTERM	AK23	IN
VCTERM	VCTERM	AK27	IN
VREFA0		L31	IN
VREFA1		L27	IN
VREFC0		AD31	IN
VREFC1		AD27	IN
VREFDL0		AD23	IN
VREFDL1		AD19	IN
VREFDR0		L23	IN
VREFDR1		L19	IN

Table 3-2. Pin/Signal Information Sorted by Pin Location

Pin Name	System Bus Signal Name	Pin Location	Input/Output
GND	GND	A01	IN
PROCPRES#	CPUPRES#	A03	OUT
OUTEN	OUTEN	A05	IN
N/C		A07	
N/C		A09	
GND	GND	A11	IN
AP1#	AP1#	A13	IN/OUT
A12#	AA12#/BE4#	A15	IN/OUT
A18#	AA18#/DID2#	A17	IN/OUT
A25#	AA25#/ATTR1#	A19	IN/OUT
A27#	AA27#/ATTR3#	A21	IN/OUT
A29#	AA29#/ATTR5#	A23	IN/OUT
A31#	AA31#/ATTR7#	A25	IN/OUT
A33#	AA33#/AB33#	A27	IN/OUT
A35#	AA35#/AB35#	A29	IN/OUT
A37#	AA37#/AB37#	A31	IN/OUT
A39#	AA39#/AB39#	A33	IN/OUT
A41#	AA41#/AB41#	A35	IN/OUT
GND	GND	A37	IN
3.3V		B02	IN
SMA0	SMA0	B04	IN
PPODGD#	PPODGD#	B06	OUT
N/C		B08	
GND	GND	B10	IN
AP0#	AP0#	B12	IN/OUT
A11#	AA11#/BE3#	B14	IN/OUT
A17#	AA17#/DID1#	B16	IN/OUT

Table 3-2. Pin/Signal Information Sorted by Pin Location (Cont'd)

Pin Name	System Bus Signal Name	Pin Location	Input/Output
A23#	AA23#/DID7#	B18	IN/OUT
A24#	AA24#/ATTR0#	B20	IN/OUT
A26#	AA26#/ATTR2#	B22	IN/OUT
A28#	AA28#/ATTR4#	B24	IN/OUT
A30#	AA30#/ATTR6#	B26	IN/OUT
A32#	AA32#/AB32#	B28	IN/OUT
A34#	AA34#/AB34#	B30	IN/OUT
A36#	AA36#/AB36#	B32	IN/OUT
A38#	AA38#/AB38#	B34	IN/OUT
A40#	AA40#/AB40#	B36	IN/OUT
A43#	AA43#/AB43#	B38	IN/OUT
3.3V		C01	IN
SMA1	SMA1	C03	IN
GND	GND	C05	IN
GND	GND	C07	IN
N/C		C09	
GND	GND	C11	IN
GND	GND	C13	IN
GND	GND	C15	IN
GND	GND	C17	IN
GND	GND	C19	IN
GND	GND	C21	IN
GND	GND	C23	IN
GND	GND	C25	IN
GND	GND	C27	IN
GND	GND	C29	IN
GND	GND	C31	IN
GND	GND	C33	IN
GND	GND	C35	IN
A42#	AA42#/AB42#	C37	IN/OUT
SMWP	SMWP	D02	IN
SMA2	SMA2	D04	IN
N/C		D06	
IGNNE#	IGNNE#	D08	IN
GND	GND	D10	IN
A06#	AA06#/EXF3#/FCL#/SPLCK#	D12	IN/OUT
A10#	AA10#/BE2#	D14	IN/OUT
A16#	AA16#/DID0#	D16	IN/OUT
A22#	AA22#/DID6#	D18	IN/OUT
D31#	D31#	D20	IN/OUT
D29#	D29#	D22	IN/OUT
D27#	D27#	D24	IN/OUT
D25#	D25#	D26	IN/OUT
DEP2#	DEP2#	D28	IN/OUT
STBN1#	STBN1#	D30	IN/OUT

Table 3-2. Pin/Signal Information Sorted by Pin Location (Cont'd)

Pin Name	System Bus Signal Name	Pin Location	Input/Output
D23#	D23#	D32	IN/OUT
D21#	D21#	D34	IN/OUT
D19#	D19#	D36	IN/OUT
D17#	D17#	D38	IN/OUT
SMSD	SMSD	E01	IN/OUT
VCTERM	VCTERM	E03	IN
N/C		E05	
VCTERM	VCTERM	E07	IN
LINT1	NMI	E09	IN
GND	GND	E11	IN
GND	GND	E13	IN
GND	GND	E15	IN
GND	GND	E17	IN
VCTERM	VCTERM	E19	IN
GND	GND	E21	IN
VCTERM	VCTERM	E23	IN
GND	GND	E25	IN
VCTERM	VCTERM	E27	IN
GND	GND	E29	IN
GND	GND	E31	IN
GND	GND	E33	IN
GND	GND	E35	IN
GND	GND	E37	IN
SMSC	SMSC	F02	IN
N/C		F04	
THERMTRIP#	THERMTRIP#	F06	OUT
LINT0	INT	F08	IN
GND	GND	F10	IN
A05#	AA05#/EXF2#/OWN#	F12	IN/OUT
A09#	AA09#/BE1#	F14	IN/OUT
A15#	AA15#/BE7#	F16	IN/OUT
A21#	AA21#/DID5#	F18	IN/OUT
D30#	D30#	F20	IN/OUT
D28#	D28#	F22	IN/OUT
D26#	D26#	F24	IN/OUT
D24#	D24#	F26	IN/OUT
DEP3#	DEP3#	F28	IN/OUT
STBP1#	STBP1#	F30	IN/OUT
D22#	D22#	F32	IN/OUT
D20#	D20#	F34	IN/OUT
D18#	D18#	F36	IN/OUT
D16#	D16#	F38	IN/OUT
GND	GND	G01	IN
THRMALERT#	THRMALERT#	G03	OUT
GND	GND	G05	IN

Table 3-2. Pin/Signal Information Sorted by Pin Location (Cont'd)

Pin Name	System Bus Signal Name	Pin Location	Input/Output
GND	GND	G07	IN
N/C		G09	
GND	GND	G11	IN
GND	GND	G13	IN
GND	GND	G15	IN
GND	GND	G17	IN
VCTERM	VCTERM	G19	IN
GND	GND	G21	IN
VCTERM	VCTERM	G23	IN
GND	GND	G25	IN
VCTERM	VCTERM	G27	IN
GND	GND	G29	IN
GND	GND	G31	IN
GND	GND	G33	IN
GND	GND	G35	IN
GND	GND	G37	IN
N/C		H02	
PD0		H04	
N/C		H06	
A20M#	A20M#	H08	IN
GND	GND	H10	IN
A04#	AA04#/EXF1#/DEN#	H12	IN/OUT
A08#	AA08#/BE0#	H14	IN/OUT
A14#	AA14#/BE6#	H16	IN/OUT
A20#	AA20#/DID4#	H18	IN/OUT
D15#	D15#	H20	IN/OUT
D13#	D13#	H22	IN/OUT
D11#	D11#	H24	IN/OUT
D09#	D09#	H26	IN/OUT
STBP0#	STBP0#	H28	IN/OUT
DEP1#	DEP1#	H30	IN/OUT
D07#	D07#	H32	IN/OUT
D05#	D05#	H34	IN/OUT
D03#	D03#	H36	IN/OUT
D01#	D01#	H38	IN/OUT
N/C		J01	
VCTERM	VCTERM	J03	IN
N/C		J05	
VCTERM	VCTERM	J07	IN
FERR#	FERR#	J09	OUT
GND	GND	J11	IN
GND	GND	J13	IN
GND	GND	J15	IN
GND	GND	J17	IN
VCTERM	VCTERM	J19	IN

Table 3-2. Pin/Signal Information Sorted by Pin Location (Cont'd)

Pin Name	System Bus Signal Name	Pin Location	Input/Output
GND	GND	J21	IN
VCTERM	VCTERM	J23	IN
GND	GND	J25	IN
VCTERM	VCTERM	J27	IN
GND	GND	J29	IN
GND	GND	J31	IN
GND	GND	J33	IN
GND	GND	J35	IN
GND	GND	J37	IN
N/C		K02	
N/C		K04	
N/C		K06	
N/C		K08	
GND	GND	K10	IN
A03#	AA03#/EXF0#/DPS#	K12	IN/OUT
A07#	AA07#/EXF4#	K14	IN/OUT
A13#	AA13#/BE5#	K16	IN/OUT
A19#	AA19#/DID3#	K18	IN/OUT
D14#	D14#	K20	IN/OUT
D12#	D12#	K22	IN/OUT
D10#	D10#	K24	IN/OUT
D08#	D08#	K26	IN/OUT
STBN0#	STBN0#	K28	IN/OUT
DEP0#	DEP0#	K30	IN/OUT
D06#	D06#	K32	IN/OUT
D04#	D04#	K34	IN/OUT
D02#	D02#	K36	IN/OUT
D00#	D00#	K38	IN/OUT
GND	GND	L01	IN
N/C		L03	
GND	GND	L05	IN
N/C		L07	
GND	GND	L09	IN
GND	GND	L11	IN
GND	GND	L13	IN
GND	GND	L15	IN
GND	GND	L17	IN
VREFDR1		L19	IN
GND	GND	L21	IN
VREFDR0		L23	IN
GND	GND	L25	IN
VREFA1		L27	IN
GND	GND	L29	IN
VREFA0		L31	IN
GND	GND	L33	IN

Table 3-2. Pin/Signal Information Sorted by Pin Location (Cont'd)

Pin Name	System Bus Signal Name	Pin Location	Input/Output
GND	GND	L35	IN
GND	GND	L37	IN
GND	GND	AD01	IN
N/C		AD03	
GND	GND	AD05	IN
N/C		AD07	
GND	GND	AD09	IN
BR2#	BREQ2#	AD11	IN
DBSY#	DBSY#	AD13	IN/OUT
DRDY#	DRDY#	AD15	IN/OUT
REQ1#	WSNP#, D/C#/LEN1#	AD17	IN/OUT
VREFDL1		AD19	IN
GND	GND	AD21	IN
VREFDL0		AD23	IN
GND	GND	AD25	IN
VREFC1		AD27	IN
GND	GND	AD29	IN
VREFC0		AD31	IN
GND	GND	AD33	IN
GND	GND	AD35	IN
GND	GND	AD37	IN
N/C		AE02	
N/C		AE04	
TRISTATE#	TRISTATE#	AE06	IN
N/C		AE08	
HITM#	HITM#	AE10	IN/OUT
HIT#	HIT#	AE12	IN/OUT
REQ4#	ASZ1#/DSZ1#	AE14	IN/OUT
DEFER#	DEFER#	AE16	IN
TRDY#	TRDY#	AE18	IN
D48#	D48#	AE20	IN/OUT
D50#	D50#	AE22	IN/OUT
D52#	D52#	AE24	IN/OUT
D54#	D54#	AE26	IN/OUT
STBN3#	STBN3#	AE28	IN/OUT
DEP7#	DEP7#	AE30	IN/OUT
D56#	D56#	AE32	IN/OUT
D58#	D58#	AE34	IN/OUT
D60#	D60#	AE36	IN/OUT
D62#	D62#	AE38	IN/OUT
PD1		AF01	
VCTERM	VCTERM	AF03	IN
N/C		AF05	
VCTERM	VCTERM	AF07	IN
GND	GND	AF09	IN

Table 3-2. Pin/Signal Information Sorted by Pin Location (Cont'd)

Pin Name	System Bus Signal Name	Pin Location	Input/Output
GND	GND	AF11	IN
GND	GND	AF13	IN
GND	GND	AF15	IN
GND	GND	AF17	IN
VCTERM	VCTERM	AF19	IN
GND	GND	AF21	IN
VCTERM	VCTERM	AF23	IN
GND	GND	AF25	IN
VCTERM	VCTERM	AF27	IN
GND	GND	AF29	IN
GND	GND	AF31	IN
GND	GND	AF33	IN
GND	GND	AF35	IN
GND	GND	AF37	IN
N/C		AG02	
N/C		AG04	
TRST#	TRST#	AG06	IN
N/C		AG08	
BR0#	BREQ0#	AG10	IN/OUT
REQ3#	ASZ0#/DSZ0#	AG12	IN/OUT
RS2#	RS2#	AG14	IN
LOCK#	LOCK#	AG16	IN/OUT
ADS#	ADS#	AG18	IN/OUT
D49#	D49#	AG20	IN/OUT
D51#	D51#	AG22	IN/OUT
D53#	D53#	AG24	IN/OUT
D55#	D55#	AG26	IN/OUT
STBP3#	STBP3#	AG28	IN/OUT
DEP6#	DEP6#	AG30	IN/OUT
D57#	D57#	AG32	IN/OUT
D59#	D59#	AG34	IN/OUT
D61#	D61#	AG36	IN/OUT
D63#	D63#	AG38	IN/OUT
GND	GND	AH01	IN
N/C		AH03	
GND	GND	AH05	IN
PMI#	PMI#	AH07	IN
GND	GND	AH09	IN
GND	GND	AH11	IN
GND	GND	AH13	IN
GND	GND	AH15	IN
GND	GND	AH17	IN
VCTERM	VCTERM	AH19	IN
GND	GND	AH21	IN
VCTERM	VCTERM	AH23	IN

Table 3-2. Pin/Signal Information Sorted by Pin Location (Cont'd)

Pin Name	System Bus Signal Name	Pin Location	Input/Output
GND	GND	AH25	IN
VCTERM	VCTERM	AH27	IN
GND	GND	AH29	IN
GND	GND	AH31	IN
GND	GND	AH33	IN
GND	GND	AH35	IN
GND	GND	AH37	IN
TUNER2		AJ02	IN
N/C		AJ04	IN
TDI	TDI	AJ06	IN
N/C		AJ08	
BR1#	BREQ1#	AJ10	IN
RSP#	RSP#	AJ12	IN
RS0#	RS0#	AJ14	IN
REQ0#	REQA0#/LEN0#	AJ16	IN/OUT
BNR#	BNR#	AJ18	IN/OUT
D32#	D32#	AJ20	IN/OUT
D34#	D34#	AJ22	IN/OUT
D36#	D36#	AJ24	IN/OUT
D38#	D38#	AJ26	IN/OUT
DEP4#	DEP4#	AJ28	IN/OUT
STBP2#	STBP2#	AJ30	IN/OUT
D40#	D40#	AJ32	IN/OUT
D42#	D42#	AJ34	IN/OUT
D44#	D44#	AJ36	IN/OUT
D46#	D46#	AJ38	IN/OUT
PD2		AK01	
VCTERM	VCTERM	AK03	IN
N/C		AK05	
VCTERM	VCTERM	AK07	IN
GND	GND	AK09	IN
GND	GND	AK11	IN
GND	GND	AK13	IN
GND	GND	AK15	IN
GND	GND	AK17	IN
VCTERM	VCTERM	AK19	IN
GND	GND	AK21	IN
VCTERM	VCTERM	AK23	IN
GND	GND	AK25	IN
VCTERM	VCTERM	AK27	IN
GND	GND	AK29	IN
GND	GND	AK31	IN
GND	GND	AK33	IN
GND	GND	AK35	IN
GND	GND	AK37	IN

Table 3-2. Pin/Signal Information Sorted by Pin Location (Cont'd)

Pin Name	System Bus Signal Name	Pin Location	Input/Output
TUNER1		AL02	
N/C		AL04	
TDO	TDO	AL06	OUT
N/C		AL08	
BR3#	BREQ3#	AL10	IN
RP#	RP#	AL12	IN/OUT
REQ2#	REQA2#/ REQB2#	AL14	IN/OUT
BPRI#	BPRI#	AL16	IN
BERR#	BERR#	AL18	IN/OUT
D33#	D33#	AL20	IN/OUT
D35#	D35#	AL22	IN/OUT
D37#	D37#	AL24	IN/OUT
D39#	D39#	AL26	IN/OUT
DEP5#	DEP5#	AL28	IN/OUT
STBN2#	STBN2#	AL30	IN/OUT
D41#	D41#	AL32	IN/OUT
D43#	D43#	AL34	IN/OUT
D45#	D45#	AL36	IN/OUT
D47#	D47#	AL38	IN/OUT
PD3		AM01	
N/C		AM03	
GND	GND	AM05	IN
TMS	TMS	AM07	IN
GND	GND	AM09	IN
GND	GND	AM11	IN
GND	GND	AM13	IN
GND	GND	AM15	IN
GND	GND	AM17	IN
GND	GND	AM19	IN
GND	GND	AM21	IN
GND	GND	AM23	IN
GND	GND	AM25	IN
GND	GND	AM27	IN
GND	GND	AM29	IN
GND	GND	AM31	IN
GND	GND	AM33	IN
GND	GND	AM35	IN
BCLKN	BCLKN	AM37	IN
N/C		AN02	
N/C		AN04	
TCK	TCK	AN06	IN
N/C		AN08	
PU0		AN10	
RS1#	RS1#	AN12	IN
BINIT#	BINIT#	AN14	IN/OUT

Table 3-2. Pin/Signal Information Sorted by Pin Location (Cont'd)

Pin Name	System Bus Signal Name	Pin Location	Input/Output
RESET#	RESET#	AN16	IN
GSEQ#	GSEQ#	AN18	IN
BPM4#	BPM4#	AN20	IN/OUT
BPM2#	BPM2#	AN22	IN/OUT
BPM0#	BPM0#	AN24	IN/OUT
IDS#	IDS#	AN26	IN
ID6#	IDA6#/IDB6#	AN28	IN
ID4#	IDA4#/IDB4#	AN30	IN
ID2#	IDA2#/DHIT#	AN32	IN
SBSY#	SBSY#	AN34	IN/OUT
DRATE#	DRATE#	AN36	IN
BCLKP	CLK	AN38	IN
GND	GND	AP01	IN
PU1		AP03	
PWRGOOD	PWRGOOD	AP05	IN
INIT#	INIT#	AP07	IN
GND	GND	AP09	IN
PU2		AP11	
GND	GND	AP13	IN
GND	GND	AP15	IN
GND	GND	AP17	IN
BPM5#	BPM5#	AP19	IN/OUT
BPM3#	BPM3#	AP21	IN/OUT
BPM1#	BPM1#	AP23	IN/OUT
TND#	TND#	AP25	IN/OUT
ID7#	IDA7#/IDB7#	AP27	IN
ID5#	IDA5#/IDB5#	AP29	IN
ID3#	IDA3#/IDB3#	AP31	IN
ID1#	IDA1#/IP1#	AP33	IN
ID0#	IDA0#/IP0#	AP35	IN
GND	GND	AP37	IN

Mechanical Specifications 4

This chapter provides the mechanical specifications of the Intel Itanium processor PAC418 (418 pin array cartridge) package.

4.1 Cartridge Features

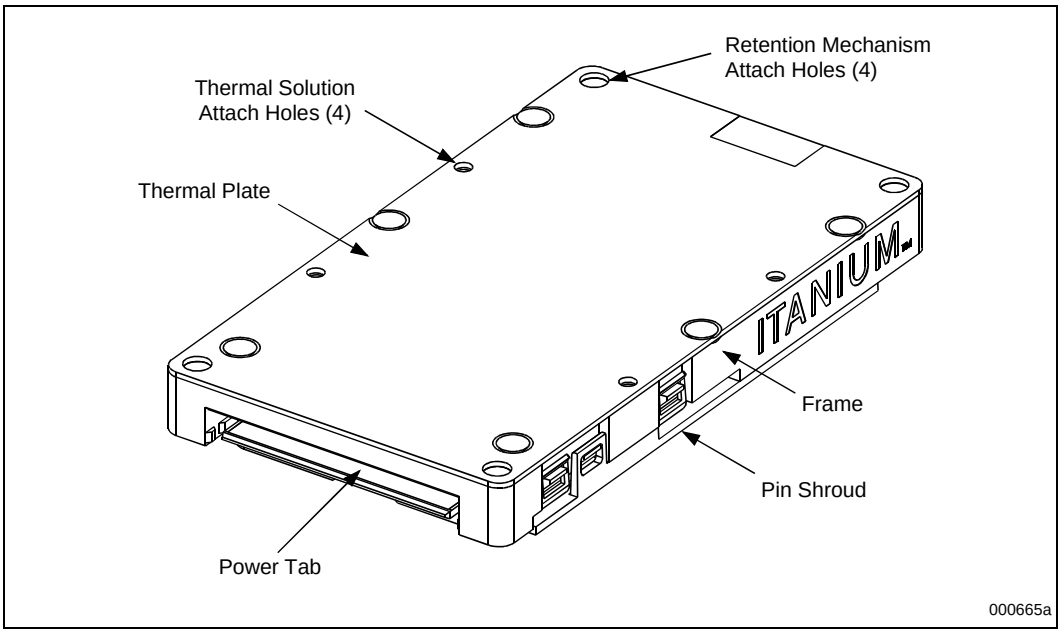
The PAC418 package contains the Intel Itanium processor core, L3 cache, and other passive components. The PAC418 cartridge connects to the motherboard through a PAC418 socket. The Intel Itanium processor 4-MB and 2-MB cartridges have identical footprints and are mechanically identical. The top of the cartridge is the thermal plate to which a cooling solution is attached. This side of the cartridge has two sets of holes, one set for retention mechanism attachment and another set for cooling solution attachment. The bottom side of the cartridge contains the pin array, pin shroud, and the alignment pegs/keys. One end of the cartridge has the power tab interface to connect with the Power Pod. The other end of the cartridge has an identification label. Table 4-1 contains the dimensions for the PAC418 cartridge.

4.1.1 Cartridge Top Surface Features

Figure 4-1 shows the top view of the Intel Itanium processor PAC418 cartridge. The diagram illustrates the cartridge cooling solution and retention mechanism attachment feature details on the thermal plate (the retention mechanism is the mechanical component designed to hold the socketed processor and power pod to the baseboard and socket and the thermal plate is the surface used to connect a heatsink or other thermal solution to the processor). Four holes with M2.5x0.45 threads are used to attach the cartridge cooling solution to the thermally active region of the cartridge which is represented by the hashed region in Figure 4-7. Please refer to *Itanium™ Processor Heatsink Guidelines* for more information on the heatsink specifications.

Also shown in Figure 4-1 is the retention mechanism attachment through holes which are used to interface with the mechanical support posts on the retention mechanism. Please refer to *PAC418 Cartridge/Power Pod Retention Mechanism and Triple Beam Design Specifications* for more information on the retention mechanism. A plastic frame surrounds the sides of the cartridge and the pin shroud surrounds the cartridge pins. The power tab (the power connector located on one end of the cartridge which connects to the power pod) is used to interface with the Power Pod which supplies power to the components inside the PAC418 cartridge.

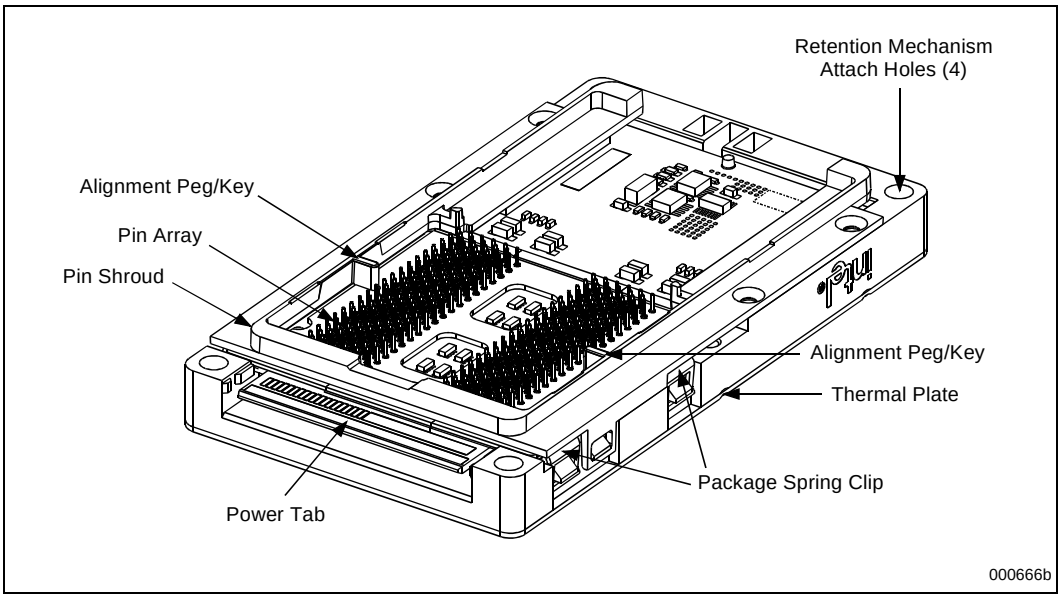
Figure 4-1. Intel® Itanium™ Processor PAC418 Top Isometric View



4.1.2 Cartridge Bottom Surface Features

Figure 4-2 shows the bottom view of the PAC418 cartridge. The cartridge pins are surrounded by a pin shroud which protects the pins. The shroud is taller than the PAC418 pins so the cartridge can rest on the shroud without damage to the pins. Two alignment pegs/keys extend from the shroud to ensure correct cartridge pin and socket alignment during the socketing process. The pegs/keys are slightly offset with respect to one another and serve as a keying feature. Please refer to *PAC418 VLIF Socket and Cartridge Ejector Design Specifications* for more information on the pin shroud and cartridge pin alignment.

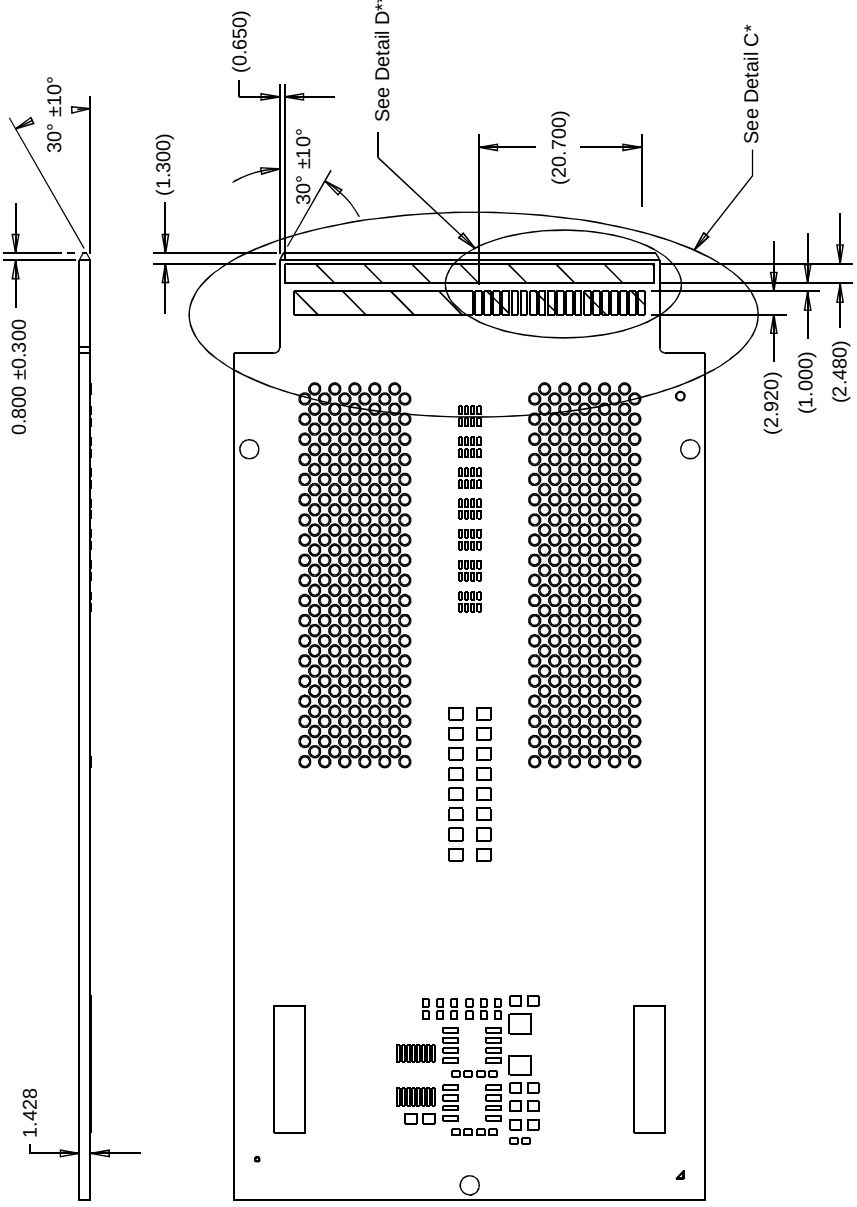
Figure 4-2. Intel® Itanium™ Processor PAC418 Bottom Isometric View



4.1.3 Power Connector

The Power Pod will deliver power to the PAC418 cartridge through the power tab. Figure 4-3 through Figure 4-8 illustrate the dimensions and characteristics of the power tab area located on the PAC418 cartridge substrate.

Figure 4-3. Power Tab Location on PAC418 Cartridge Substrate



Bottom view of substrate (cartridge body not shown for clarity).
Dimensions are in millimeters.
*Refer to Figure 4-7.
**Refer to Figure 4-8.

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Figure 4-4. Power Tab Location on PAC418 Cartridge Substrate, Detail C

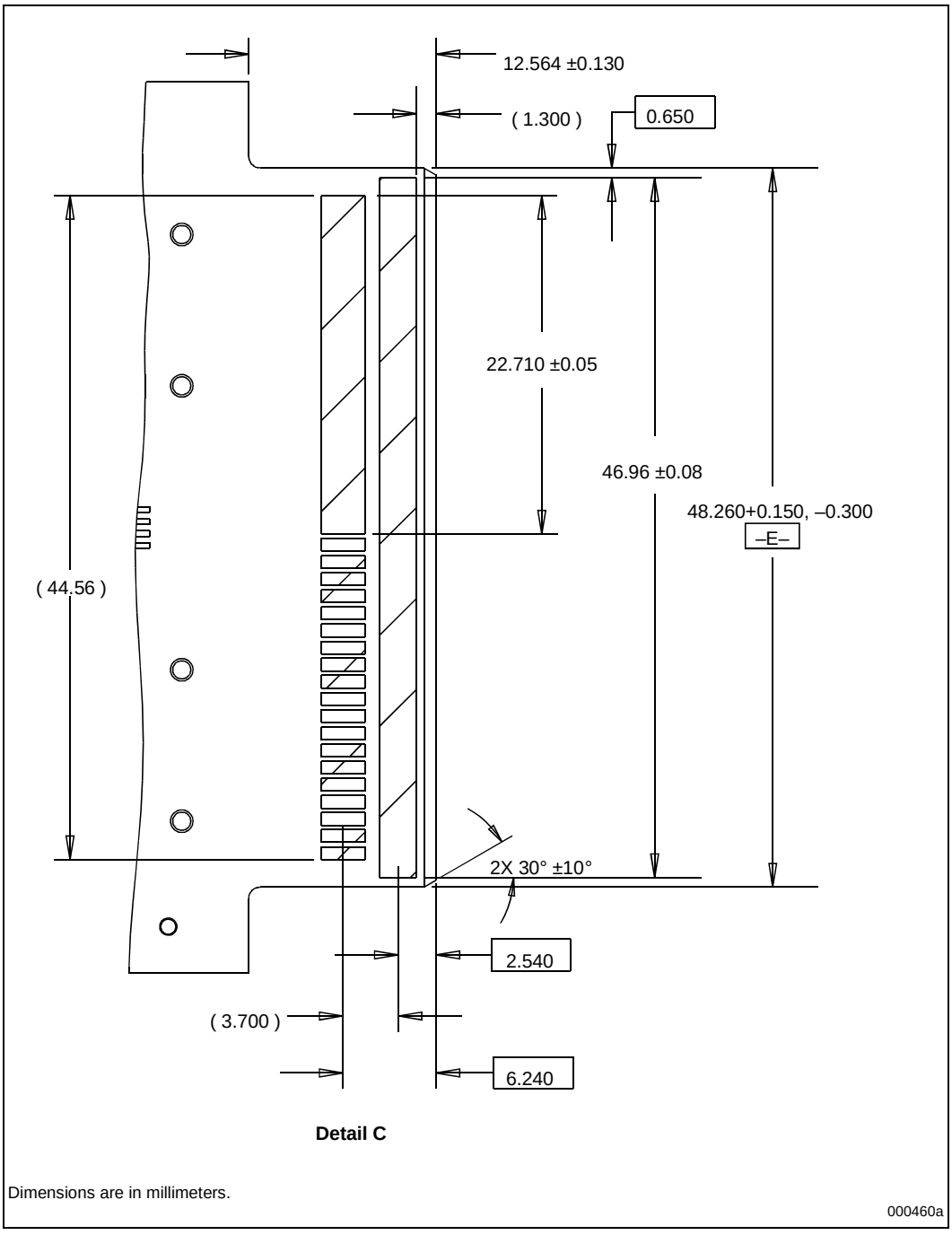
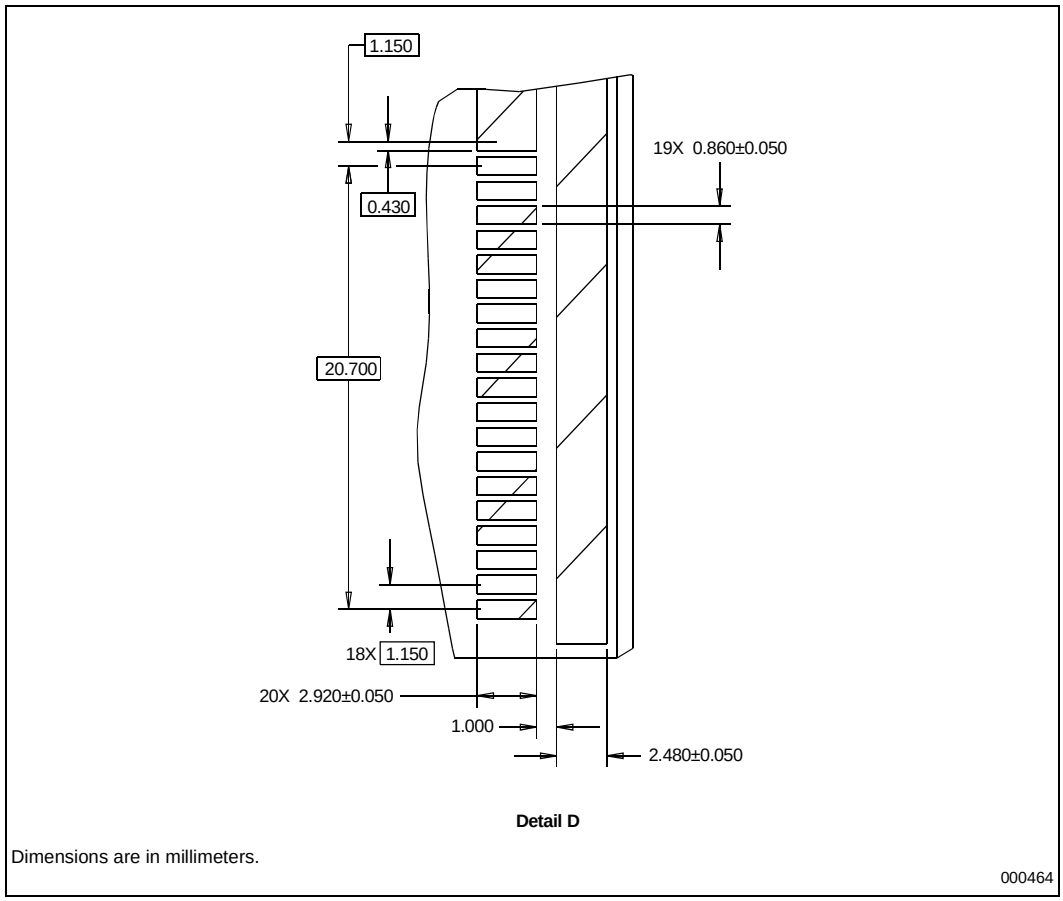


Figure 4-5. Power Tab Location on PAC418 Cartridge Substrate, Detail D



4.2 Cartridge Mechanical Dimensions

Figure 4-6, Figure 4-7, and Figure 4-8 show the top, bottom, side, and both end views of the Intel Itanium processor PAC418 cartridge. Figure 4-1 and Figure 4-2 show the top and bottom isometric views of the cartridge with key features identified.

The following notes apply to Figure 4-6, Figure 4-7, and Figure 4-8. Unless otherwise specified:

1. Interpret dimensions and tolerances in accordance with ASME Y14.5M-1994.
2. Dimensions are in INCHES.
3. Tolerance: .XX±.01, .XXX±.005, Angles: ±3 degrees.

Table 4-1 contains detailed cartridge dimensions to be used in conjunction of Figure 4-6 through Figure 4-8.

The following notes apply to Table 4-1 unless otherwise specified.

1. [ ] brackets signify a basic dimension, a dimension from which other dimensions are based.
2. ( ) brackets signify a reference dimension, a dimension that is used as reference information.
3. Dimensions that are not enclosed in brackets are actual dimensions with tolerances.

Figure 4-6. Intel® Itanium™ Processor PAC418 Cartridge Mechanical Drawings (Sheet 1 of 3)

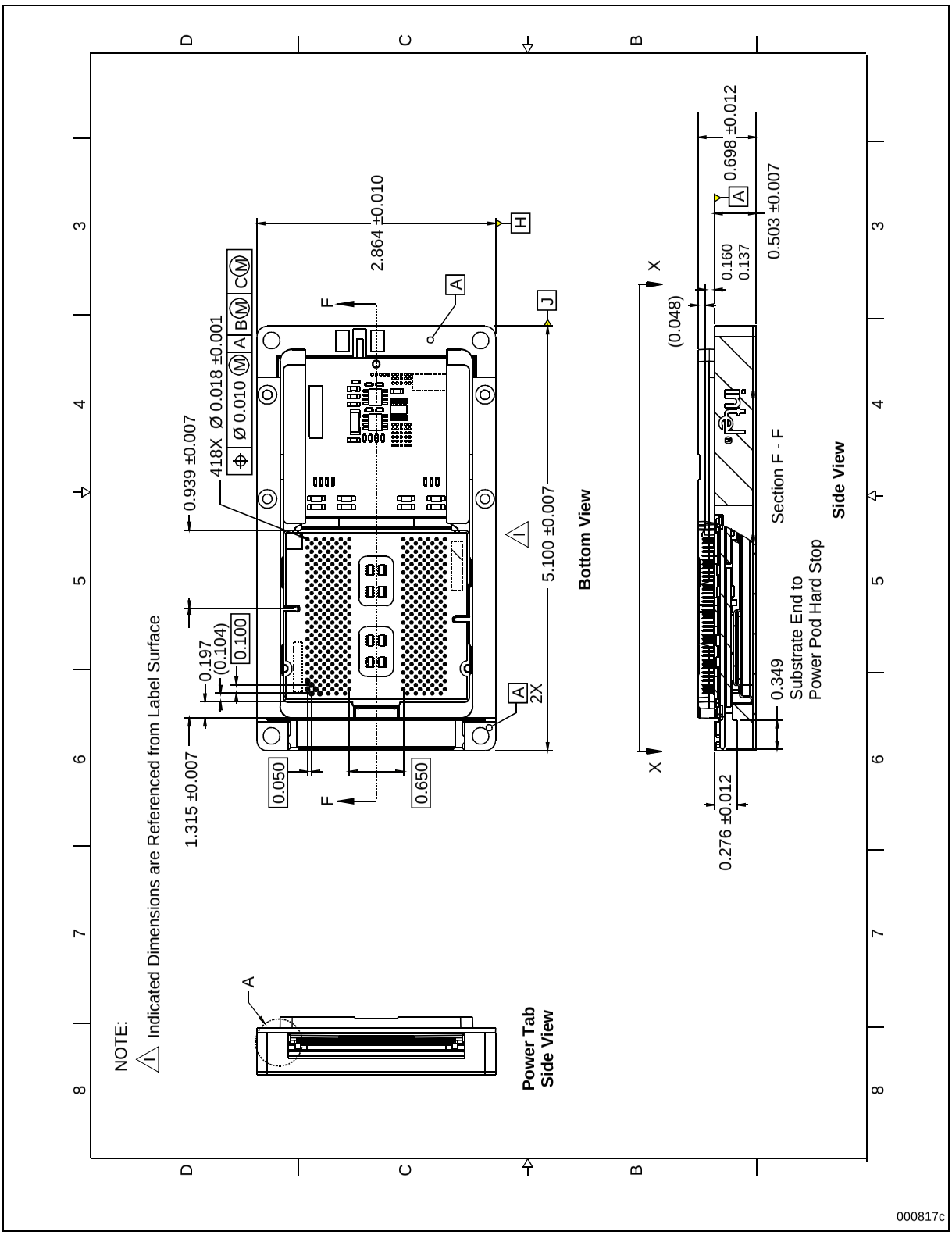


Figure 4-7. Intel® Itanium™ Processor PAC418 Cartridge Mechanical Drawings (Sheet 2 of 3)

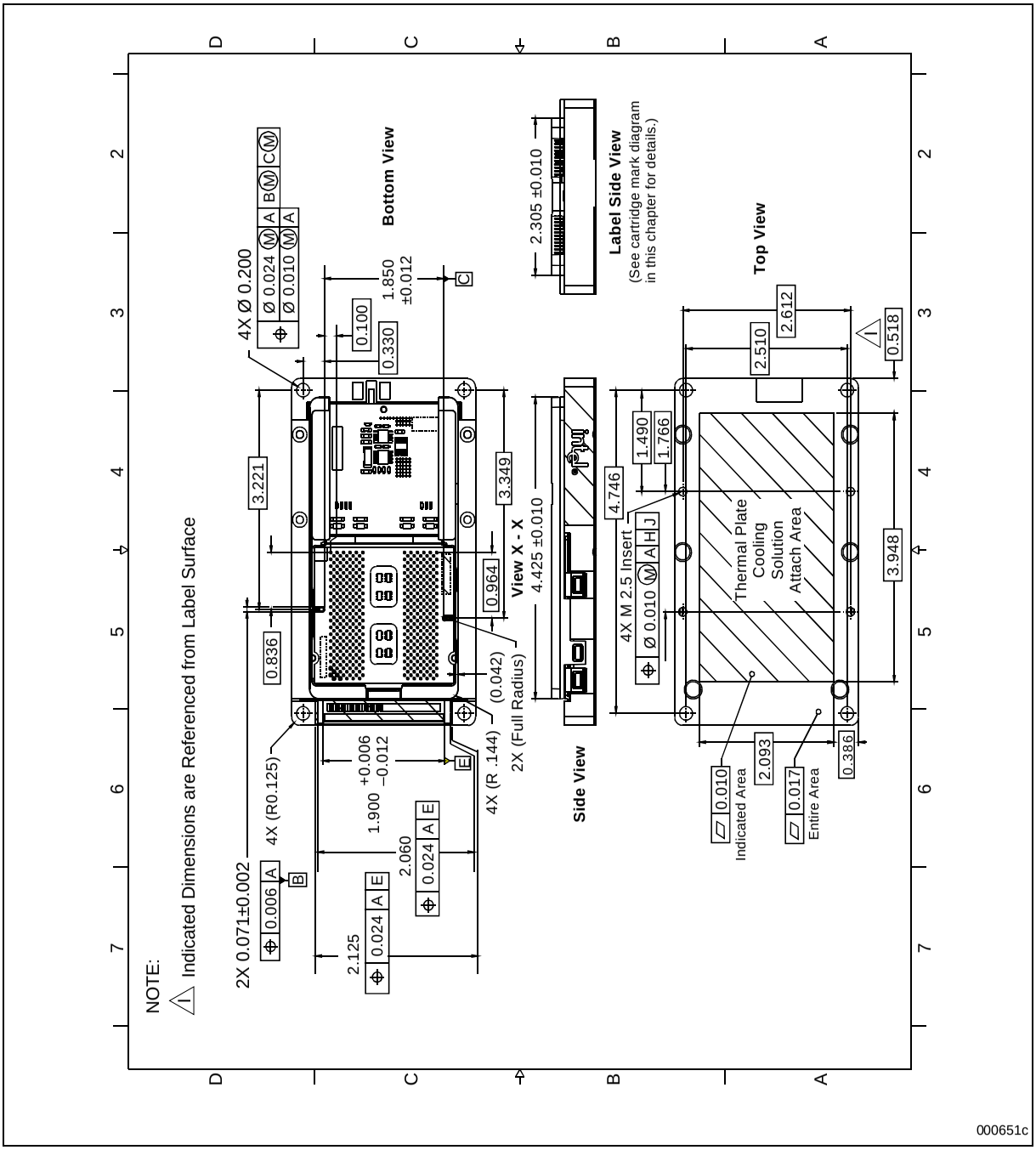


Figure 4-8. Intel® Itanium™ Processor PAC418 Cartridge Mechanical Drawings (Sheet 3 of 3)

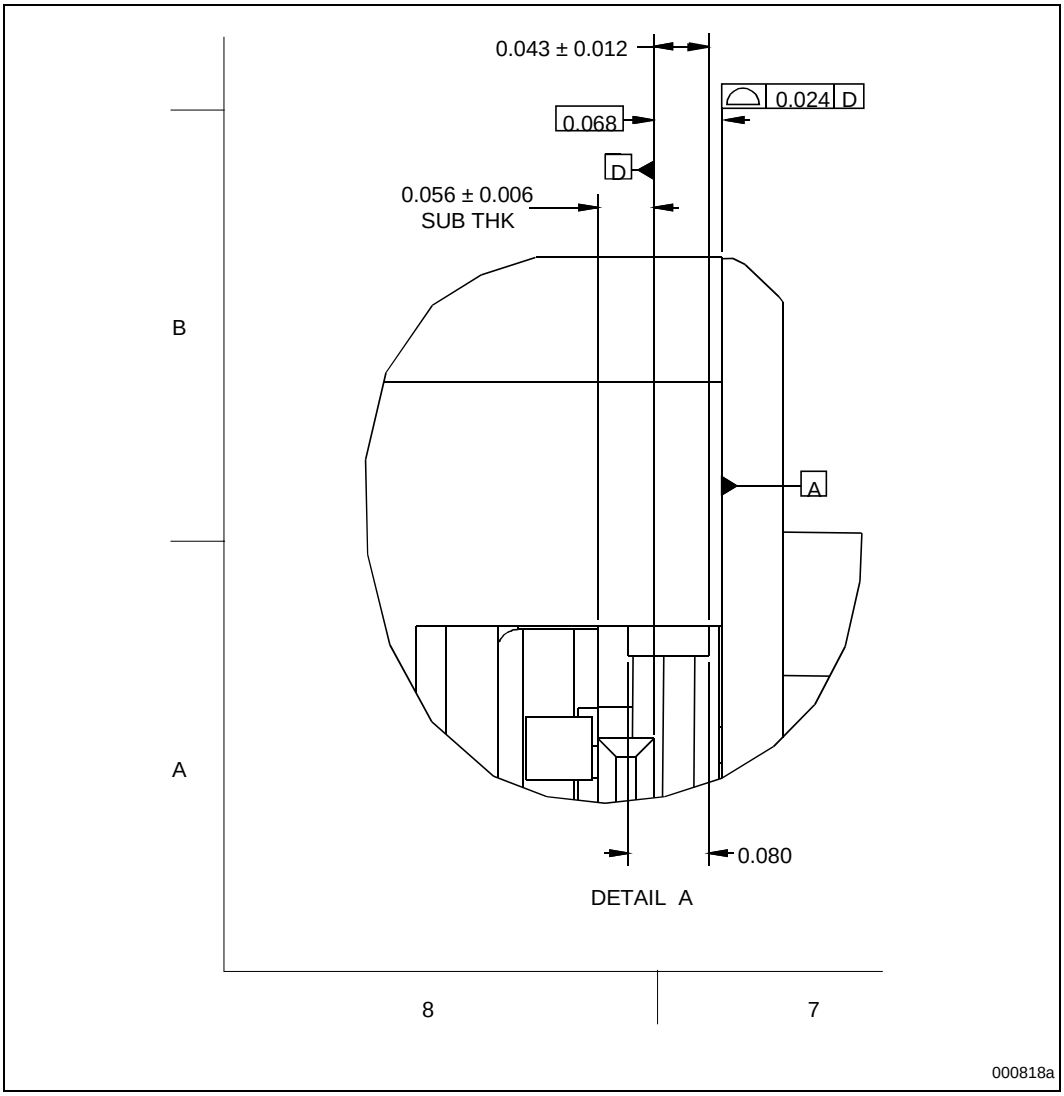


Table 4-1. Intel® Itanium™ Processor PAC418 Cartridge Dimensions

Dimension Description	Drawing Location (Sheet #- Coordinates)	Value (Inches)	Metric Reference Value (mm)
Cartridge Length (including label)	1-B5	5.100±.007	129.54±.18
Pin Protector Length (Outer)	2-C4	4.425±.010	112.40±.25
Cartridge Width	1-C3	2.864±.0010	72.75±.25
Pin Protector Width (Outer)	2-C2	2.305±.010	58.55±.25
Cartridge Thickness	1-B3	0.698±.012	17.73±.30
Body Thickness	1-A3	0.503±.007	12.78±.18
Cartridge RM Attach Hole Spacing Length (Basic)	2-B4	[4.746]	[120.55]
Cartridge RM Attach Hole Spacing Width (Basic)	2-A3	[2.510]	[63.75]
Cartridge RM Attach Hole Diameter	2-D3	0.200±.005	5.08±.13
Cartridge RM Attach Hole True Position wrt Datums A, B, and C	2-D3	0.024	0.61
Cartridge RM Attach Hole True Position wrt Datum A	2-D3	0.010	0.25
Thermal Solution Attachment Insert Thread Size (Reference)	2-B5	M2.5x0.45	M2.5x0.45
Thermal Solution Attachment Insert True Position	2-B5	0.010	0.25
Maximum Thermal Solution Screw Engagement Depth from Top Surface of Cartridge (Reference)		(0.394)	(10.01)
Pin Row Group Center Spacing (Basic)	1-C6	[0.650]	[16.51]
Pin Pitch Row to Row (Basic)	1-D6	[0.050]	[1.27]
Pin Protector to Pin CL Spacing (Reference)	1-D5	(0.104)	(2.64)
Top Alignment Key to Pin Protector	1-D6	1.315±.007	33.40±.18
Top Alignment Key to Pin Protector Feature	1-D4	0.939±.007	23.85±.18
Pin Pitch Within Row (Basic)	1-D5	[0.100]	[2.54]
Pin Protector Wall Width	1-D5	0.197±.005	5.00±.13
Thermal Solution Attachment Hole to RM Attach Hole (Basic)	2-B4	[1.490]	[37.85]
Thermal Solution Attachment Hole Spacing Length (Basic)	2-B5	[1.766]	[44.86]
Thermal Solution Attachment Hole Spacing Width (Basic)	2-A3	[2.612]	[66.34]
Top Alignment Key to RM Attach Hole (Basic)	2-D4	[3.221]	[81.81]
Bottom Key to RM Attach Hole (Basic)	2-C4	[3.349]	[85.06]
Top Alignment Key to Pin 1 (Basic)	2-D4	[0.836]	[21.23]
Bottom Alignment Key to Pin 1 (Basic)	2-C4	[0.964]	[24.49]
Alignment Key Width	2-D7	0.071±.002	1.80±.05
Alignment Key Width True Position	2-D7	0.006	.15
Alignment Key to RM Attach Hole (Basic)	2-D3	[0.330]	[8.38]
Alignment Key to Pin 1 (Basic)	2-D3	[0.100]	[2.54]

Table 4-1. Intel® Itanium™ Processor PAC418 Cartridge Dimensions (Cont'd)

Dimension Description	Drawing Location (Sheet #- Coordinates)	Value (Inches)	Metric Reference Value (mm)
Alignment Key to Alignment Key	2-D3	1.850±.012	46.99±.30
Pin Diameter	1-D4	0.018±.001	0.46±.025
Pin Tip True Position	1-D4	0.010	0.25
Thermal Solution Attach Area Length (Basic)	2-A5	[3.948]	[100.28]
Thermal Solution Attach Area Width (Basic)	2-A6	[2.093]	[53.16]
Thermal Solution Attach Area Length Offset (Basic)	2-A3	[0.518]	[13.16]
Thermal Solution Attach Area Width Offset (Basic)	2-A6	[0.386]	[9.80]
Power Pod Connector Opening Height wrt Datum A	1-B6	0.276±.012	7.01±.30
Power Pod Connector Opening Width	2-D7	2.125±.005	53.98±.13
Power Pod Connector Opening Width True Position	2-D7	0.024	0.61
Power Pod Connector Rail to Rail	2-C7	2.060±.005	52.32±.13
Power Pod Connector Rail wrt Substrate True Position	2-C7	0.024	0.61
Power Tab Substrate Width	2-C6	1.900+.006,-.012	48.26+.15,-.30
Substrate End to Power Pod Connector Hard Stop	1-A6	0.349±.005	8.86±.13
Cartridge Radius (Reference)	2-D6	(0.125)	(3.18)
Pin Protector Radius (Reference)	2-C6	(0.144)	(3.66)
Alignment Key Radius (Reference)	2-C5	Full Radius	Full Radius
Pin Protector Wall Width (Reference)	2-C5	(0.042)	(1.07)
Pin Length wrt Datum A (Max/Min)	1-B3	0.160/0.137	4.06/3.48
Pin Protector Height to Pin Tip (Reference)	1-B3	(0.048)	(1.22)
Cartridge Top Surface Flatness	2-A6	0.017	0.38
Cartridge Top Surface Thermal Solution Attach Area Flatness	2-B6	0.010	0.25
Power Tab Substrate Thickness	3-B8	0.056±.006	1.42±.15
Datum D to Datum A (Basic)	3-B8	[0.068]	[1.73]
Datum D to Datum A Profile Tolerance	3-B7	0.024	0.61
Datum D to Power Pod Connector Rail	3-B8	0.043±.012	1.09±.30
Power Pod Connector Rail Thickness	3-A7	0.080±.005	2.03±.13

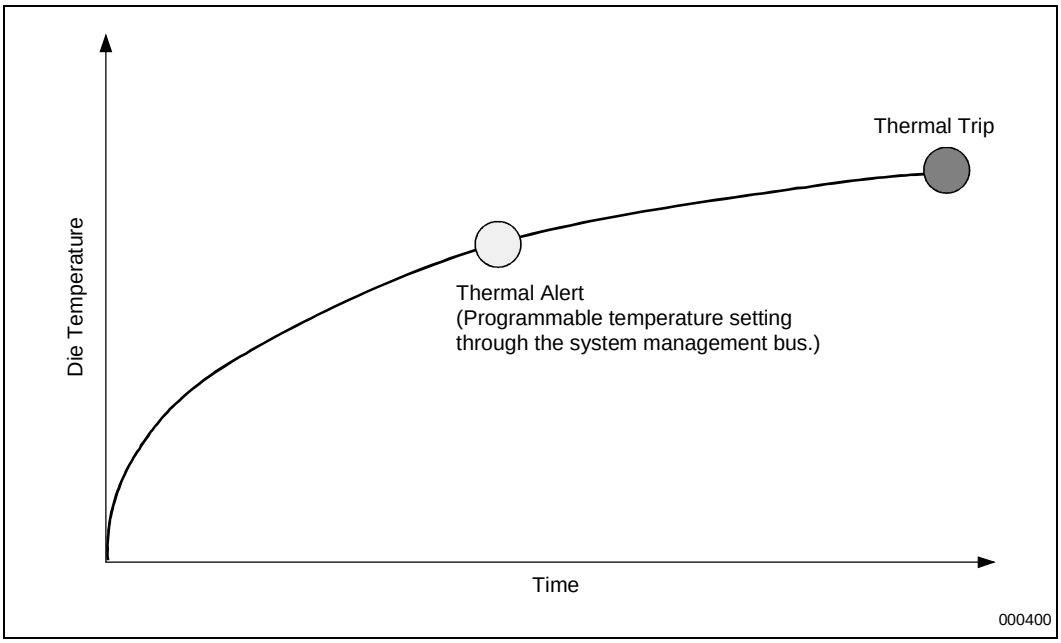
Thermal Specifications 5

This chapter provides a description of the thermal diode features and thermal data relating to the Intel Itanium processor.

5.1 Thermal Circuit

The Intel Itanium processor has an internal thermal circuit which senses when a certain temperature is reached on the die. This circuit is used for thermal trip. In addition, an on-chip thermal diode is available for use by the thermal sensing device on the Intel Itanium processor cartridge. Figure 5-1 highlights the relative positions of the Intel Itanium processor thermal features.

Figure 5-1. Intel® Itanium™ Processor Thermal Features



5.1.1 Thermal Alert

THRMALERT# is a programmable thermal alert signal which is one of the Intel Itanium processor cartridge system management features. THRMALERT# is asserted when the measured temperature from the processor thermal diode equals or exceeds the temperature threshold data programmed in the high-temp (T_{high}) register on the sensor (see Chapter 6 for more details). This signal can be used by the platform to implement thermal regulation features such as generating an external interrupt to tell the system management software that the processor core die temperature is increasing.

5.1.2 Thermal Trip

The Intel Itanium processor protects itself from catastrophic overheating by use of an internal thermal sensor. The sensor trip-point is set well above the normal operating temperature to ensure that there are no false trips. The Intel Itanium processor will stop all execution when the junction temperature exceeds a safe operating level. *Data will be lost if the Intel Itanium processor goes into thermal trip (signaled to the system by the THRMTRIP# pin).* Once thermal trip is activated, the Intel Itanium processor remains stopped until RESET# is asserted. If the die temperature has dropped below the trip level, a RESET# pulse can be used to reset the processor. If the temperature has not dropped below the trip level, the processor will continue to drive THRMTRIP# and remain stopped.

5.2 Cartridge Thermal Specifications and Considerations

This section lists the thermal parameters of the Intel Itanium processor cartridge. Systems should be designed to dissipate a maximum power consumption of 130W from each Intel Itanium processor cartridge.

5.2.1 Thermal Plate Temperature

To ensure functional and reliable Intel Itanium processor operation, the thermal plate temperature (T_{plate}) must be maintained within the T_{plate} temperature specifications in Table 5-1.

Table 5-1. Intel® Itanium™ Processor Thermal Design Specifications

Processor Core Frequency (MHz)	L3 Cache Size (MB)	Max Total Cartridge Power (P_{MAX})	Minimum T_{plate} (°C)	Maximum T_{plate} (°C)
733 / 800 MHz	2	116.0W	5.0	66.0
	4	130.0W	5.0	66.0

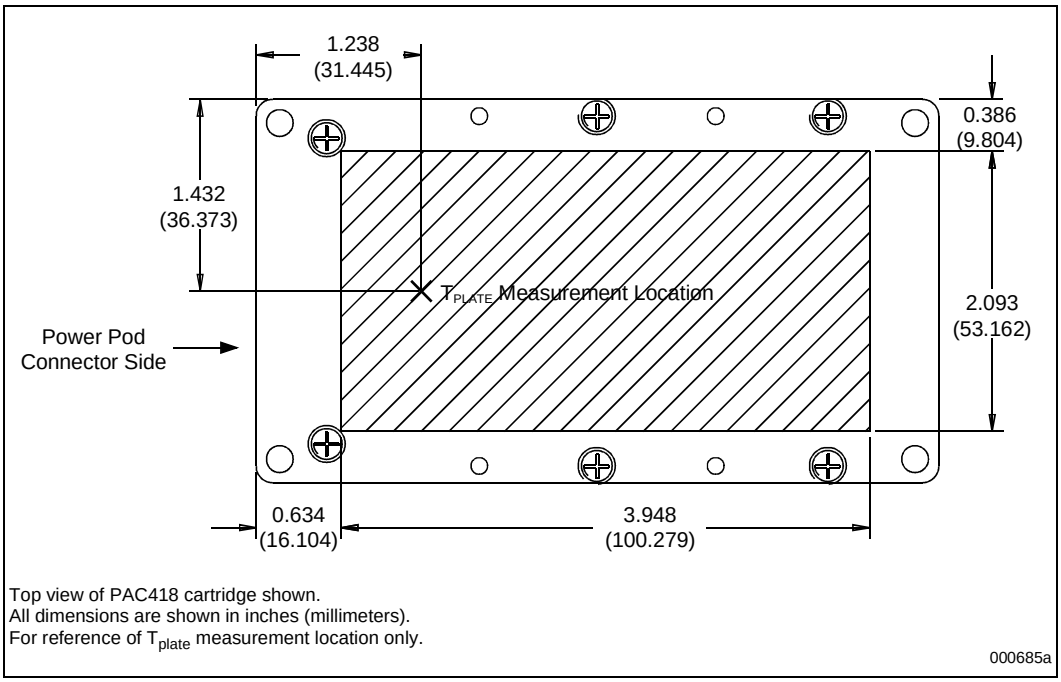
5.2.2 Thermal Budget

All processor thermal solutions should attach to the thermal plate.

The thermal solution must adequately control the thermal plate temperature below the maximum and above the minimum specified in Table 5-1. The performance of any thermal solution is defined as the thermal resistance between the thermal plate and the ambient air around the processor (Θ_{PA}). The lower the thermal resistance between the thermal plate and the ambient air, the more efficient the thermal solution. The required Θ_{PA} is dependent upon the maximum allowed thermal plate temperature (T_{plate}), the local ambient temperature (T_{LA}), and the maximum cartridge power (P_{MAX}).

$$\Theta_{PA} = (T_{plate} - T_{LA})/P_{MAX}$$

Figure 5-2. Processor T_{plate} Temperature Measurement Location



The Θ_{PA} value is made up of two primary components: the thermal resistance between the thermal plate and heatsink (Θ_{PA}) and the thermal resistance between the heatsink and the ambient air around the processor (Θ_{HA}). One factor to consider in decreasing Θ_{PA} is the thermal interface between the thermal plate and the cooling solution. The other controllable factor (Θ_{HA}) is resultant in the design of the heatsink and airflow around the heatsink. Heatsink design constraints are also provided in *Itanium™ Processor Heatsink Guidelines*.

The maximum T_{plate} and the thermal plate power are listed in Table 5-1. T_{LA} is a function of the system design. Table 5-2 provides the resultant thermal solution performance for a 733 MHz/ 800 MHz Intel Itanium processor at different ambient air temperatures around the processor.

Table 5-2. Example Thermal Solution Performance for the 4MB Intel® Itanium™ Processor Cartridge at Thermal Plate Power of 130W

Thermal Solution (Performance)	Local Ambient Temperature (T_{LA})		
	35°C	40°C	45°C
Θ_{PA} (°C/W)	0.24	0.20	0.16

5.2.3 Cartridge Temperature Deviation

The maximum temperature deviation (ΔT_{MAX}) across the top surface of the cartridge in the thermal active area is 10°C.

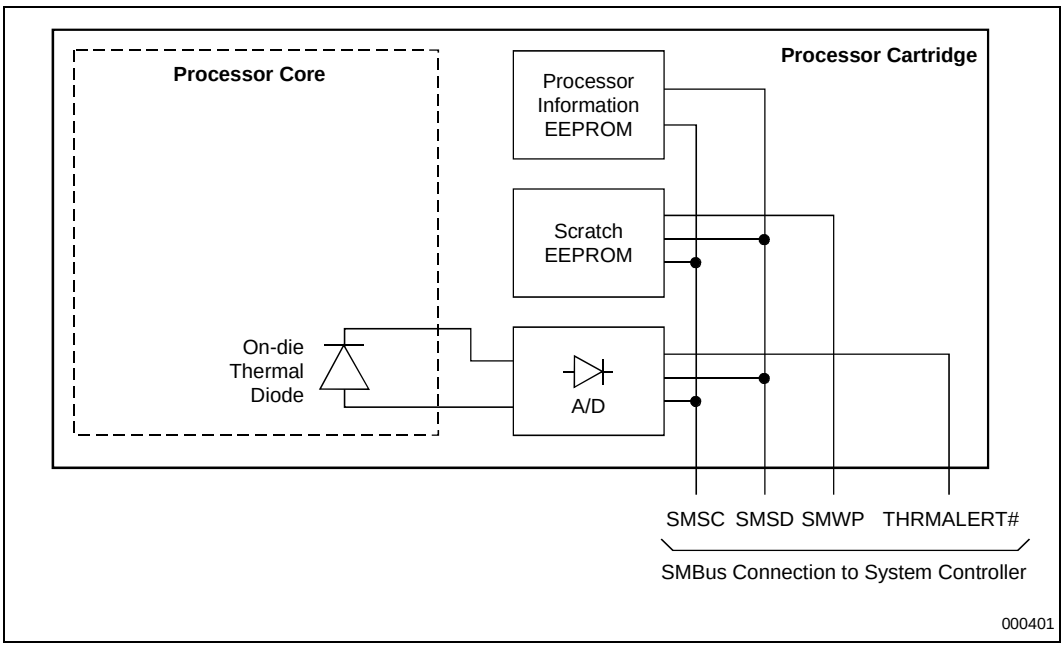
System Management Feature Specifications 6

This Intel Itanium processor includes a System Management Bus (SMBus) interface. This chapter describes the features of the SMBus and SMBus components.

6.1 System Management Features and Components

The Intel Itanium processor have several built-in components to aid in the system management. These components include a thermal sensor (digital thermometer), a Processor Information EEPROM (PIROM) and a Scratch EEPROM as shown in Figure 6-1. The PIROM is programmed by Intel with information specific to manufacturing and features of the Itanium processor cartridge. This information is permanently write-protected. The Scratch EEPROM is available for the OEM system designers to use at their discretion. The thermal sensor can be used in conjunction with the information in the PIROM and/or the Scratch EEPROM for system thermal monitoring and management. The thermal sensor on the cartridge provides an accurate means of acquiring the relative junction temperature of the processor core die. The thermal sensing device is connected to the anode and cathode of the processor's on-die thermal diode.

Figure 6-1. System Management Components on the Intel® Itanium™ Processor Cartridge



6.2 System Management Interface

6.2.1 SMBus Signals

Table 6-1 lists the System Management Interface signals and their descriptions. These signals are used by the system to access the system management components via the SMBus. The SMBus implementation on the Itanium processor cartridge uses the clock and data signals of the SMBus specifications in Table 2-16.

Table 6-1. System Management Interface Signal Descriptions

Signal Name	Pin Count	Description
3.3V	2	Voltage supply for EEPROMs and thermal sensor
SMA[2:0]	3	System Management address bus
SMSC	1	System Management bus clock
SMSD	1	System Management serial address/data bus
SMWP	1	Scratch EEPROM write protect
THRMALERT#	1	Temperature alert from the thermal sensor

Figure 6-2 is a logical schematics of SMBus circuitry on the Intel Itanium processor cartridge and shows how the various system management components are connected to the SMBus. The reference to the System Board at the lower left corner of the figure shows how SMBus address configuration for multiple Itanium processors can be realized with resistor stuffing options.

Note: Actual implementation of SMBus on the OEM platforms may differ from this implementation. This figure is meant to be used in general understanding of the Itanium processor SMBus architecture.

6.2.2 SMBus Device Addressing

Of the addresses broadcast across the SMBus, the memory components claim those of the form “1010XXYZb”. The “XX” and “Y” bits are used to enable the devices on the cartridge at adjacent addresses. The Y bit is hard-wired on the cartridge to VSS (‘0’) for the Scratch EEPROM and pulled to 3.3V (‘1’) for the Processor Information ROM. The “XX” bits are defined by the processor slot via the SMA0 and SMA1 pins on the Intel Itanium processor cartridge connector. These address pins are pulled down weakly (10 kΩ) to ensure that the memory components are in a known state in systems which do not support the SMBus, or only support a partial implementation. The “Z” bit is the read/write bit for the serial bus transaction.

The thermal sensing device internally decodes one of three upper address patterns from the bus of the form “0011XXXZb”, “1001XXXZb” or “0101XXXZb”. The device’s addressing, as implemented, uses SMA2 and SMA1 and includes a Hi-Z state for the SMA2 address pin. Therefore the thermal sensing device supports six unique resulting addresses. To set the Hi-Z state for SMA2, the pin must be left floating. The system should drive SMA1 and SMA0, and will be pulled low (if not driven) by the 10 kΩ pull-down resistor on the processor substrate. Attempting to drive either of these signals to a Hi-Z state would cause ambiguity in the memory device address decode, possibly resulting in the devices not responding, thus timing out or hanging the SMBus. As before, the “Z” bit is the read/write bit for the serial bus transaction.

Figure 6-2 shows a logical diagram of the pin connections. Table 6-2 and Table 6-3 describe the address pin connections and how they affect the addressing of the devices.

Note: Addresses of the form “0000XXXXb” are Reserved and should not be generated by an SMBus master. Also, system management software must be aware of the cartridge number-dependent changes in the address for the thermal sensing device.

Figure 6-2. Logical Schematic of SMBus Circuitry

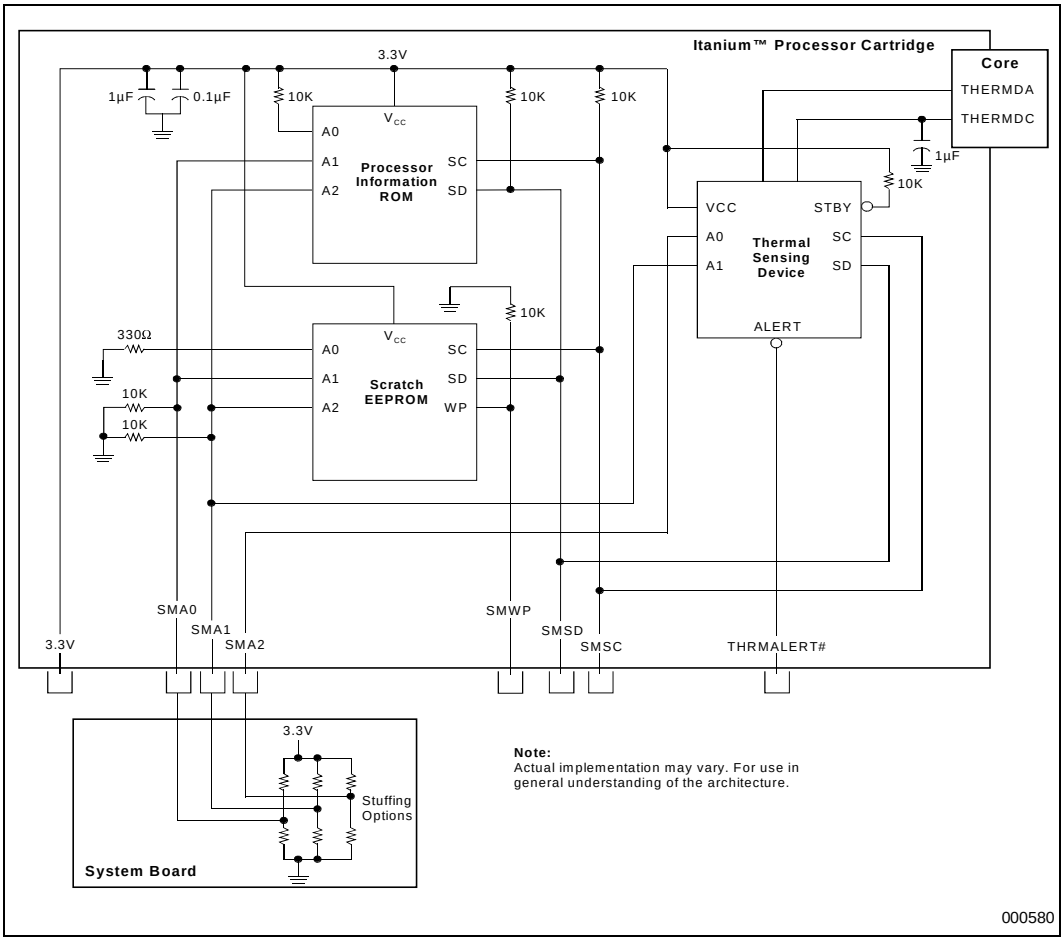


Table 6-2. Thermal Sensing Device SMBus Addressing on the Intel® Itanium™ Processor Cartridge

Address (Hex)	Upper Address[a]	Cartridge Select		8-bit Address Word on Serial Bus
		SMA1	SMA2	b[7:0]
3Xh	0011	0	0	0011000Xb
	0011	1	0	0011010Xb
5Xh	0101	0	Z[b]	0101001Xb
	0101	1	Z[b]	0101011Xb
9Xh	1001	0	1	1001100Xb
	1001	1	1	1001110Xb

a. Upper address bits are decoded in conjunction with the select pins.
b. A tri-state or “Z” state on this pin is achieved by leaving this pin unconnected.

Table 6-3. EEPROM SMBus Addressing on the Intel® Itanium™ Processor Cartridge

Address (Hex)	Upper Address[a]	Cartridge Select		Memory Device Select	Read/ Write	Device Addressed
	Bits 7–4	(SMA1) Bit 3	(SMA0) Bit 2	Bit 1	Bit 0	
A0h/A1h	1010	0	0	0	X	Scratch EEPROM 1
A2h/A3h	1010	0	0	1	X	Processor Information ROM 1
A4h/A5h	1010	0	1	0	X	Scratch EEPROM 2
A6h/A7h	1010	0	1	1	X	Processor Information ROM 2
A8h/A9h	1010	1	0	0	X	Scratch EEPROM 3
AAh/ABh	1010	1	0	1	X	Processor Information ROM 3
ACh/ADh	1010	1	1	0	X	Scratch EEPROM 4
AEh/AFh	1010	1	1	1	X	Processor Information ROM 4

a. Though this addressing scheme is targeted for up to 4-way MP systems, more processors can be supported by using a multiplexed (or separate) SMBus implementation.

6.3 PIROM and Scratch EEPROM

6.3.1 Processor Information ROM

An electrically programmed read-only memory provides information about the Intel Itanium processor cartridge. The checksum bits for each category provide error correction and serve as a mechanism to check whether data is corrupted or not. This information is permanently write-protected. Table 6-4 shows the data fields and formats provided in the memory.

Note: The data, in byte format, is written and read serially with the most significant bit first.

Table 6-4. Processor Information ROM Format

Offset/Section	# of Bits	Function	Notes	Values
HEADER: 00h	8	Data Format Revision	Two 4-bit hex digits	
01h-02h	16	EEPROM Size	Size in bytes, 16 bit binary number	128 bytes = 0080h, LSB at the lower address
03h	8	Processor Data Address	Byte pointer, 00h if not present	0Eh
04h	8	Processor Core Data Address	Byte pointer, 00h if not present	16h
05h	8	L3 Cache Data Address	Byte pointer, 00h if not present	26h
06h	8	Cartridge Data Address	Byte pointer, 00h if not present	33h
07h	8	Part Number Data Address	Byte pointer, 00h if not present	3Bh
08h	8	Thermal Reference Data Address	Byte pointer, 00h if not present	61h

Table 6-4. Processor Information ROM Format (Cont'd)

Offset/Section	# of Bits	Function	Notes	Values
09h	8	Feature Data Address	Byte pointer, 00h if not present	65h
0Ah	8	Other Data Address	Byte pointer, 00h if not present	79h
0Bh-0Ch	16	Reserved	Reserved for future use	
0Dh	8	Checksum	1 byte checksum	
PROCESSOR: 0Eh				
0Eh-13h	48	S-Spec/QDF Number	Six 8-bit ASCII characters	00VXYZ[a]
14h[1:0]	2	Sample/Production	00b = Sample only all others = Productions	
14h[7:2]	6	Reserved	Reserved for future use	
15h	8	Checksum	1 byte checksum	
CORE: 16h				
16h	8	Architecture Revision	From CPUID[b]	
17h	8	Processor Core Family	From CPUID[b]	
18h	8	Processor Core Model	From CPUID[b]	
19h	8	Processor Core Stepping (Revision)	From CPUID[b]	
1Ch-1Ah	24	Reserved	Reserved for future use	
1Dh-1Eh	16	Maximum Core Frequency	in MHz, 16 bit binary number	i.e. 800MHz = 0320h, LSB at the lower address
1Fh-20h[3:0]	12	Maximum System Bus Frequency	in MHz, 12 bit binary number	i.e. 133Mhz = 085h, LSB at the lower address
20h[7:4]-22h[3:0]	16	Processor Core Voltage	Voltage in mV, 16 bit binary number	i.e. 1.6V = 0640h, LSB at the lower address
22h[7:4]-23h[3:0]	8	Core Voltage Tolerance, High	Power Pod tolerance in mV, +	
23h[7:4]-24h[3:0]	8	Core Voltage Tolerance, Low	Power Pod tolerance in mV, –	
24h[7:4]-25h[3:0]	8	Reserved	Reserved for future use	
25h[7:4]-26h[3:0]	8	Checksum	1 byte checksum	
L3 CACHE: 26h				
26h[7:4]-2Ah[3:0]	32	Reserved	Reserved for future use	
2A[7:4]-2Ch[[3:0]	16	L3 Cache Size	in Kbytes, a 16 bit binary number	2MB = 0800h, 4MB = 1000h, LSB written at the lower address
2Ch[7:4]	4	Number of SRAM Components	One 4-bit hex digit	
2Dh[3:0]	4	Reserved	Reserved for future use	

Table 6-4. Processor Information ROM Format (Cont'd)

Offset/Section	# of Bits	Function	Notes	Values
2Dh[7:4]-2Fh[3:0]	16	L3 Cache Voltage	Voltage in mV, 16 bit binary number	LSB at the lower address
2Fh[7:4]-30h[3:0]	8	L3 Cache Voltage Tolerance, High	Power Pod tolerance in mV, +	
30h[7:4]-31h[3:0]	8	L3 Cache Voltage Tolerance, Low	Power Pod tolerance in mV, –	
31h[7:4]	4	Cache Stepping ID	One 4-bit hex digit	
32h[3:0]	4	Reserved	Reserved for future use	
32h[7:4]-33h[3:0]	8	Checksum	1 byte checksum	
CARTRIDGE: 33h				
33h[7:4]-37h[3:0]	32	Cartridge Revision	Four 8-bit ASCII characters	VXYZ[c]
37h[5:4]	2	Substrate Revision Software ID	2-bit revision number	
37h[7:6]-3Ah[5:0]	24	Reserved	Reserved for future use	
3Ah[7:6]-3Bh[5:0]	8	Checksum	1 byte checksum	
PART NUMBERS: 3Bh				
3Bh[7:6]-42h[5:0]	56	Processor Part Number	Seven 8-bit ASCII characters	ABCVXYZ[d]
42h[7:6]-48h[3:0]	46	Reserved	Reserved	
48h[7:4]-60h[3:0]	192	Reserved	Reserved for future use	
60h[7:4]-61h[3:0]	8	Checksum	1 byte checksum	
THERMAL REF: 61h				
61h[7:4]-62h[3:0]	8	Upper Temp Reference Byte	See Section 6.4	[e]
62h[7:4]-64h[3:0]	16	Reserved	Reserved for future use	
64h[7:4]-65h[3:0]	8	Checksum	1 byte checksum	
FEATURES: 65h				
65h[7:4]-69h[3:0]	32	IA-32 Processor Core Feature Flags	From CPUID[b]	32 bit binary number, LSB is written at the lowest address
69h[7:4]-71h[3:0]	64	Reserved	Reserved for future use	
71h[7:4]-75h[3:0]	32	Cartridge Feature Flags	Other bits = unused [4] = Upper temp reference byte [3] = unused [2] = SCRATCH EEPROM present [1] = Core VID present [0] = L3 cache VID present	1= present, 0= not present
75h[7:4]	4	Number of Devices in TAP Chain	One 4-bit hex digit	3 = 2M cart, 5 = 4M cart
77h-76h	16	Reserved	Reserved for future use	
78h	8	Checksum	1 byte checksum	

Table 6-4. Processor Information ROM Format (Cont'd)

Offset/Section	# of Bits	Function	Notes	Values
OTHER: 79h				
7Fh-79h	56	Reserved	Reserved for future use	

a. 00VXYZ, character 0 is written at the lowest address and character Z is written at the highest address. If the number of characters is greater than four, then the first character is omitted. For example, S-Spec "SL4LT" is recorded as "L4LT" and the first character "S" is omitted:

ADDRESS	VALUE
13h	L
12h	4
11h	L
10h	T
0Fh	0
0Eh	0

b. Refer to the *IA-64 Architecture Software Developer's Manual* for details on CPUID registers.
c. VXYZ, character V is written at the lowest address and character Z is written at the highest address.
d. ABCVXYZ, character A is written at the lowest address and character Z is written at the highest address.
e. This value has no unit(s) and is not a specific junction temperature.

6.3.2 Scratch EEPROM

Also available on the SMBus interface on the cartridge is an EEPROM which may be used for other data at the system vendor's discretion. The data in this EEPROM, once programmed, can be write-protected by asserting the active-high SMWP signal.

6.3.3 Processor Information ROM and Scratch EEPROM Supported SMBUS Transactions

The PIROM and Scratch EEPROM respond to three of the SMBus read packet types: current address read, random address read, and sequential read.

Table 6-5 shows the format of the current address read SMBus packet. Table 6-6 shows the format of the random read SMBus packet.

Sequential reads may begin with a current address read or a random address read. After the SMBus host controller receives the data word, it responds with an acknowledge. This will continue until the SMBus host controller responds with a negative acknowledge and a stop. In the tables, 'S' represents the SMBus start bit, 'P' represents a stop bit, 'R' represents a read, 'W' represents a write bit, 'A' represents an acknowledge, and '///' represents a negative acknowledge. The shaded bits are transmitted by the Processor Information ROM or Scratch EEPROM and the bits that are not shaded are transmitted by the SMBus host controller. In the tables the data addresses indicate 8 bits. The SMBus host controller should transmit 8 bits, but as there are only 128 addresses, the most significant bit is a don't care.

The Scratch EEPROM responds to two write packet types: byte write and page write.

Table 6-7 shows the format of the byte write SMBus packet. The page write operates the same way as the byte write except that the SMBus Host controller does not send a stop after the first data byte and acknowledge. The Scratch EEPROM internally increments its address. The SMBus host controller continues to transmit data bytes until it terminates the sequence with a stop. All data bytes will result in an acknowledge from the Scratch EEPROM. If more than eight bytes are written, the internal address will "roll over" and the previous data will be overwritten.

Performing a write with no data loads the address from which data should be read.

The internal address counter keeps track of the address accessed during the last read or write operation, incremented by one. Address “roll over” during reads is from the last byte of the last eight byte page to the first byte of the first page. “Roll over” during writes is from the last byte of the current eight byte page to the first byte of the same page.

Table 6-5. Current Address Read SMBus Packet

S	Device Address	R/W#	A	Data	///	P
1	7 bits	1	1	8 bits	1	1

Table 6-6. Random Address Read SMBus Packet

S	Device Address	R/W#	A	Data Address	A	S	Device Address	R/W#	A	Data	///	P
1	7 bits	0	1	8 bits	1	1	7 bits	1	1	8 bits	1	1

Table 6-7. Byte Write SMBus Packet

S	Device Address	R/W#	A	Data Address	A	Data	A	P
1	7 bits	0	1	8 bits	1	8 bits	1	1

6.4 Thermal Sensing Device

The Intel Itanium processor cartridge’s thermal sensing device provides a means of acquiring thermal data from the processor. The accuracy of the thermal reading is expected to be better than ±3°C. The thermal sensing device is composed of control logic, SMBus interface logic, a precision analog to digital converter, and a precision current source. The thermal sensing device drives a small current through a thermal diode located on the processor core and measures the voltage generated across the thermal diode by the current. With this information, the thermal sensing device computes a byte of temperature data. Software running on the processor or on a micro-controller can use the temperature data from the thermal sensing device to thermally manage the system.

The thermal sensing device provides a register with a data byte (7 bits plus sign) which contains a value corresponding to the sampled output of the thermal diode in the Intel Itanium processor core. The value of the byte read from the thermal sensor gives an accurate reading of processor core temperature at the time of the reading. This data can be used in conjunction with the Upper Temperature Reference byte (provided in the Processor Information ROM) for thermal management purposes. The temperature data from the thermal sensor can be read out digitally using an SMBus read command (see Section 6.4.1). The thermal sensor starts detecting when SMBus power is applied to the processor, and resets itself at power-up.

The thermal sensing device also contains alarm registers to store upper and lower thermal reference threshold data. These values can be individually programmed on the thermal sensor. If the measured value equals or exceeds the alarm threshold value, the appropriate bit is set in the thermal sensing device status register, which is also brought out to the system bus via the THRMALERT# signal (see Section 5.1.1 for more details). At power-up, the appropriate alarm register values need to be programmed into the thermal sensing device via the SMBus. It is recommended that the upper thermal reference threshold byte (provided in the Processor Information ROM) be used for setting the upper threshold value in the alarm register.

Note: The upper temperature reference byte in the PIROM is unitless and is not any specific junction temperature. It is a value to be used as a reference. By using a value, in the T_{high} register, that is smaller than the upper temperature reference byte by a number of 10, the THRMALERT# signal will be tripped 10°C earlier than by using the reference byte unmodified.

When polling the thermal sensing device on the cartridge to read the processor temperatures, it is recommended that the polling frequency be every 0.5 to 1 second.

6.4.1 Thermal Sensing Device Supported SMBus Transactions

The thermal sensing device responds to five of the SMBus packet types: write byte, read byte, send byte, receive byte, and ARA (Alert Response Address). Table 6-8 through Table 6-12 diagram the five packet types. In these tables, 'S' represents the SMBus start bit, 'P' represents a stop bit, 'Ack' represents an acknowledge, and '///' represents a negative acknowledge. The shaded bits are transmitted by the thermal sensor and the unshaded bits are transmitted by the SMBus host controller.

Table 6-8. Write Byte SMBus Packet

S	Address	Write	Ack	Command	Ack	Data	Ack	P
1	7 bits	1	1	8 bits	1	8 bits	1	1

Table 6-9. Read Byte SMBus Packet

S	Address	Write	Ack	Command	Ack	S	Address	Read	Ack	Data	///	P
1	7 bits	1	1	8 bits	1	1	7 bits	1	1	8 bits	1	1

Table 6-10. Send Byte SMBus Packet

S	Address	Write	Ack	Command	Ack	P
1	7 bits	1	1	8 bits	1	

Table 6-11. Receive Byte SMBus Packet

S	Address	Read	Ack	Data	///	P
1	7 bits	1	1	8 bits	1	1

Table 6-12. ARA SMBus Packet

S	ARA	Read	Ack	Address	///	P
1	0001 100	1	1	1001 1011	1	1

The send byte packet is used only for sending one-shot commands. The receive byte packet accesses the register commanded by the last read byte packet. If a receive byte packet was preceded by a write byte or send byte packet more recently than a read byte packet, then the behavior is undefined.

Table 6-13 shows the encoding of the command byte. All of the commands are for reading or writing registers in the thermal sensor except the one-shot command (OSHT). The one-shot command forces the immediate start of a new voltage-to-temperature conversion cycle. If a conversion is in progress when the one-shot command is received, then the command is ignored. If the thermal sensing device is in standby mode when the one-shot command is received, a conversion is performed and the sensor returns to standby mode. If the thermal sensor is in auto-convert mode and is between conversions, then the conversion rate timer resets, and the next automatic conversion takes place after a full delay elapses.

The default command after reset is the reserved value (00h). After reset, receive byte packets will return invalid data until another command is sent to the thermal sensing device.

Table 6-13. Command Byte Bit Assignment

Register	Command	Reset State	Function
RESERVED	00h	N/A	Reserved for future use
RRT	01h	N/A	Read processor core thermal data
RS	02h	N/A	Read status byte (flags, busy signal)
RC	03h	0000 0000	Read configuration byte
RCR	04h	0000 0010	Read conversion rate byte
RESERVED	05h	0111 1111	Reserved for future use
RESERVED	06h	1100 1001	Reserved for future use
RRHL	07h	0111 1111	Read processor core thermal diode T_{HIGH} limit
RRLL	08h	1100 1001	Read processor core thermal diode T_{LOW} limit
WC	09h	N/A	Write configuration byte
WCR	0Ah	N/A	Write conversion rate byte
RESERVED	0Bh	N/A	Reserved for future use
RESERVED	0Ch	N/A	Reserved for future use
WRHL	0Dh	N/A	Write processor core thermal diode T_{HIGH} limit
WRLL	0Eh	N/A	Write processor core thermal diode T_{LOW} limit
OSHT	0Fh	N/A	One shot command (use send byte packet)
RESERVED	10h - FFh	N/A	Reserved for future use

6.4.2 Thermal Sensing Device Registers

The system management software can configure and control the thermal sensor by writing to and interacting with different registers in the thermal sensor. These registers include a Thermal Reference register, two Thermal Limit registers, a Status register, a Configuration register, a Conversion Rate register, and other reserved registers. The following subsections describe the registers in detail.

6.4.2.1 Thermal Reference Registers

The thermal sensing device has an internal thermal reference register which contains the thermal reference value read by the thermal sensing device connected to the processor core thermal diode. This value ranges from +127 to –128 decimal and is expressed as a two’s complement, eight-bit number. These registers are saturating, i.e. values above 127 are represented at 127 decimal, and values below –128 are represented as –128 decimal.

6.4.2.2 Thermal Limit Registers

The thermal sensing device has two thermal limit registers; they define high and low limits for the processor core thermal diode. The encoding for these registers is the same as for the thermal reference register. If the diode thermal value equals or exceeds one of its limits, then its alarm bit in the Status Register is triggered. This indication is also brought out to the system bus via the THRMALERT# signal.

6.4.2.3 Status Register

The status register shown in Table 6-14 indicates which (if any) thermal value thresholds have been exceeded. It also indicates if a conversion is in progress or if an open circuit has been detected in the processor core thermal diode connection. Once set, alarm bits stay set until they are cleared by a status register read. A successful read to the status register will clear any alarm bits that may have been set, unless the alarm condition persists. Note that the THRMALERT# interrupt signal is latched and is not automatically cleared when the status flag bit is cleared. The latch is cleared by sending the ARA (0001100) on the SMBus.

Table 6-14. Thermal Sensing Device Status Register

Bit	Name	Function
7 (MSB)	BUSY	A one indicates that the device's analog to digital converter is busy converting.
6	RESERVED	Reserved for future use.
5	RESERVED	Reserved for future use.
4	RHIGH	A one indicates that the processor core thermal diode high temperature alarm has activated.
3	RLOW	A one indicates that the processor core thermal diode low temperature alarm has activated.
2	OPEN	A one indicates an open fault in the connection to the processor core diode.
1	RESERVED	Reserved for future use.
0 (LSB)	RESERVED	Reserved for future use.

6.4.2.4 Configuration Register

The configuration register controls the operating mode (standby vs. auto-convert) of the thermal sensing device. Table 6-15 shows the format of the configuration register. If the RUN/STOP bit is set (high) then the thermal sensing device immediately stops converting and enters standby mode. The thermal sensing device will still perform analog-to-digital conversions in standby mode when it receives a one-shot command. If the RUN/STOP bit is clear (low) then the thermal sensor enters auto-conversion mode. The thermal sensor starts operating in free running mode, auto-converting at 0.25 Hz after power-up.

Table 6-15. Thermal Sensing Device Configuration Register

Bit	Name	Reset State	Function
7 (MSB)	RESERVED	0	Reserved for future use.
6	RUN/STOP	0	Standby mode control bit. If high, the device immediately stops converting, and enters standby mode. If low, the device converts in either one-shot or auto-convert mode, see Section 6.4.2.5
5–0	RESERVED	0	Reserved for future use.

6.4.2.5 Conversion Rate Register

The contents of the conversion rate register determine the nominal rate at which analog-to-digital conversions happen when the thermal sensing device is in auto-convert mode. Table 6-16 shows the mapping between conversion rate register values and the conversion rate. As indicated in Table 6-13, the conversion rate register is set to its default state of 02h (0.25 Hz nominally) when the thermal sensing device is powered up. There is a ±25% error tolerance between the conversion rate indicated in the conversion rate register and the actual conversion rate.

Table 6-16. Thermal Sensing Device Conversion Rate Register

Register Contents	Conversion Rate (Hz)
00h	0.0625
01h	0.125
02h	0.25
03h	0.5
04h	1
05h	2
06h	4
07h	8
08h to FFh	Reserved for future use